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MS-7A15

ATX:226*173
Ver: 10

Intel -SkyLake-S plamform

CPU:

LGA1151
CPU POWER PAK *3 Phase
GT POWER PAK *2 Phase

System Chipset:

SPT-H :H110

Onboard Chip:

HD Audio Codec: ALC887
SIO: NCT5563D
Flash ROM: SPI 64 MB
DP to VGA: ITE6515

PWM:

VCORE - RT3606
DDR - RT8231
DDR VPP25- MP2143
PCH(1.0V) - RT8125E
VCCSA - RT8125E
VCCIO - MP5077(Load Switch)

Main Memory:


DDR4 * 2 (Dual Channel)

ACPI:

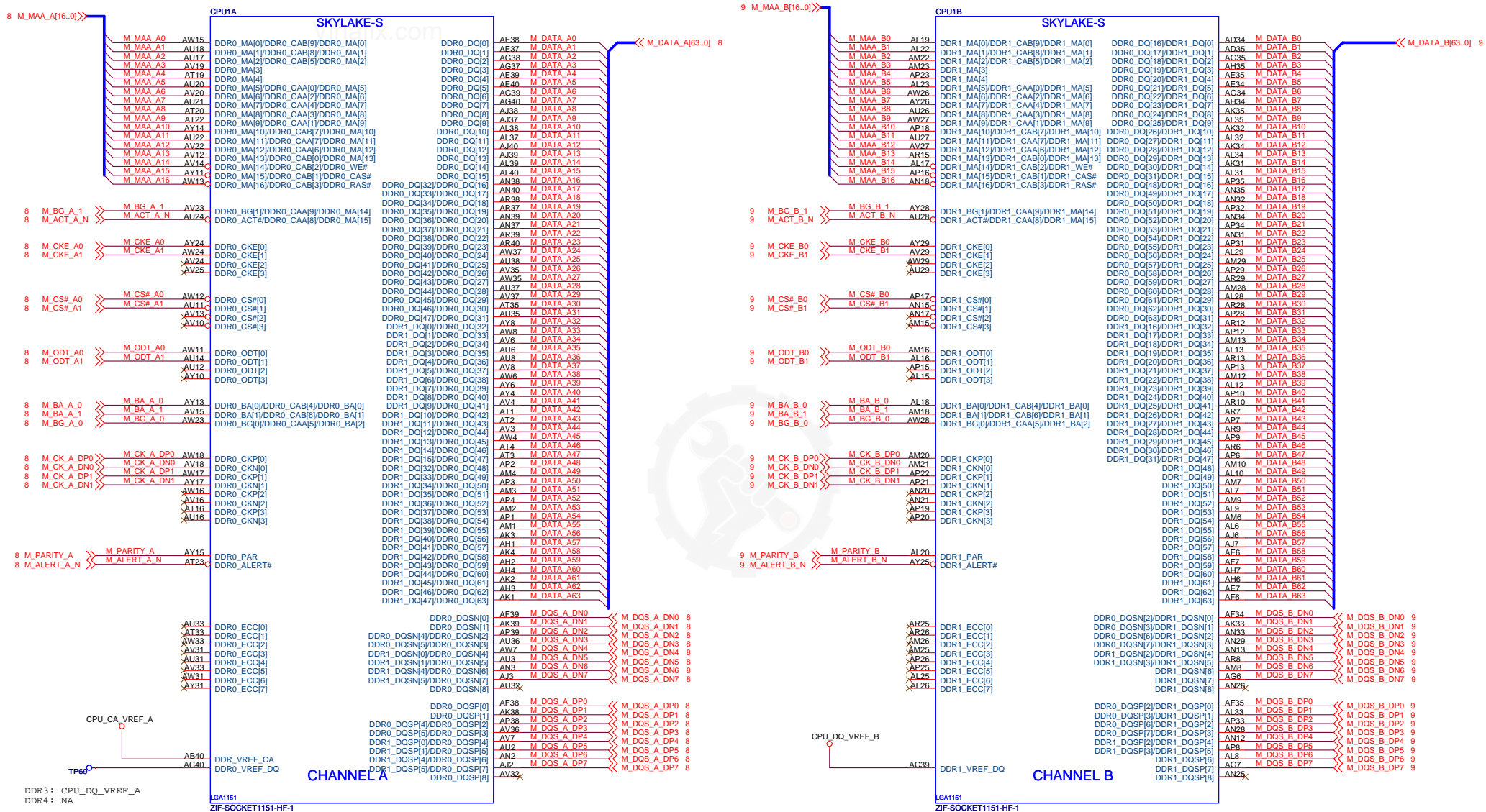
5VDAUL:uP7501 VCCSTPLL - NMOS
5VDIMM:uP7501
3VSB:GS7133
3VDSW:GS7116

Expansion Slots:

PCI Express (X16) Slot * 1
PCI Express (X1) Slot * 2



| | | |
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| MS-7A15 | | |
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See Page11 circuit



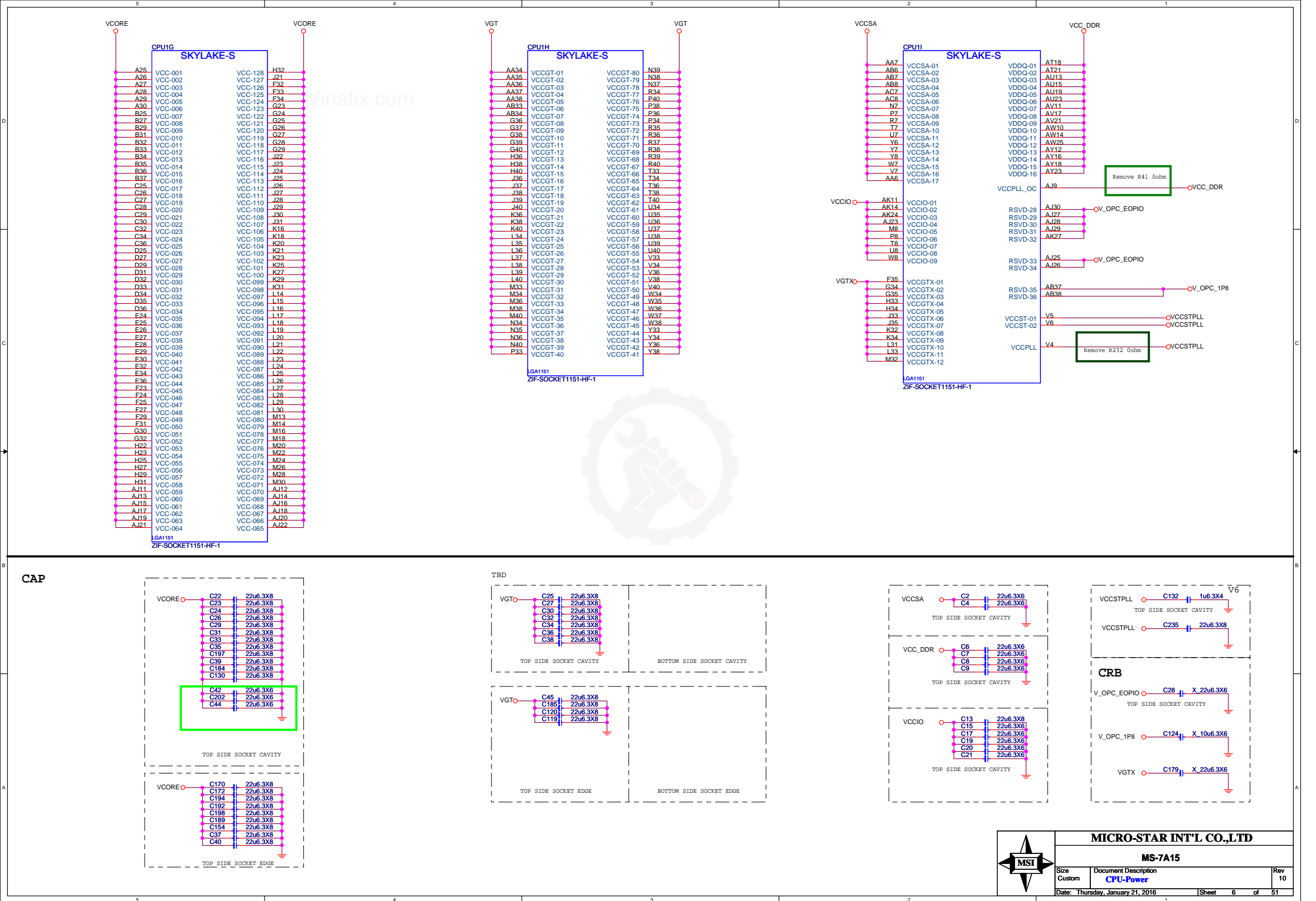
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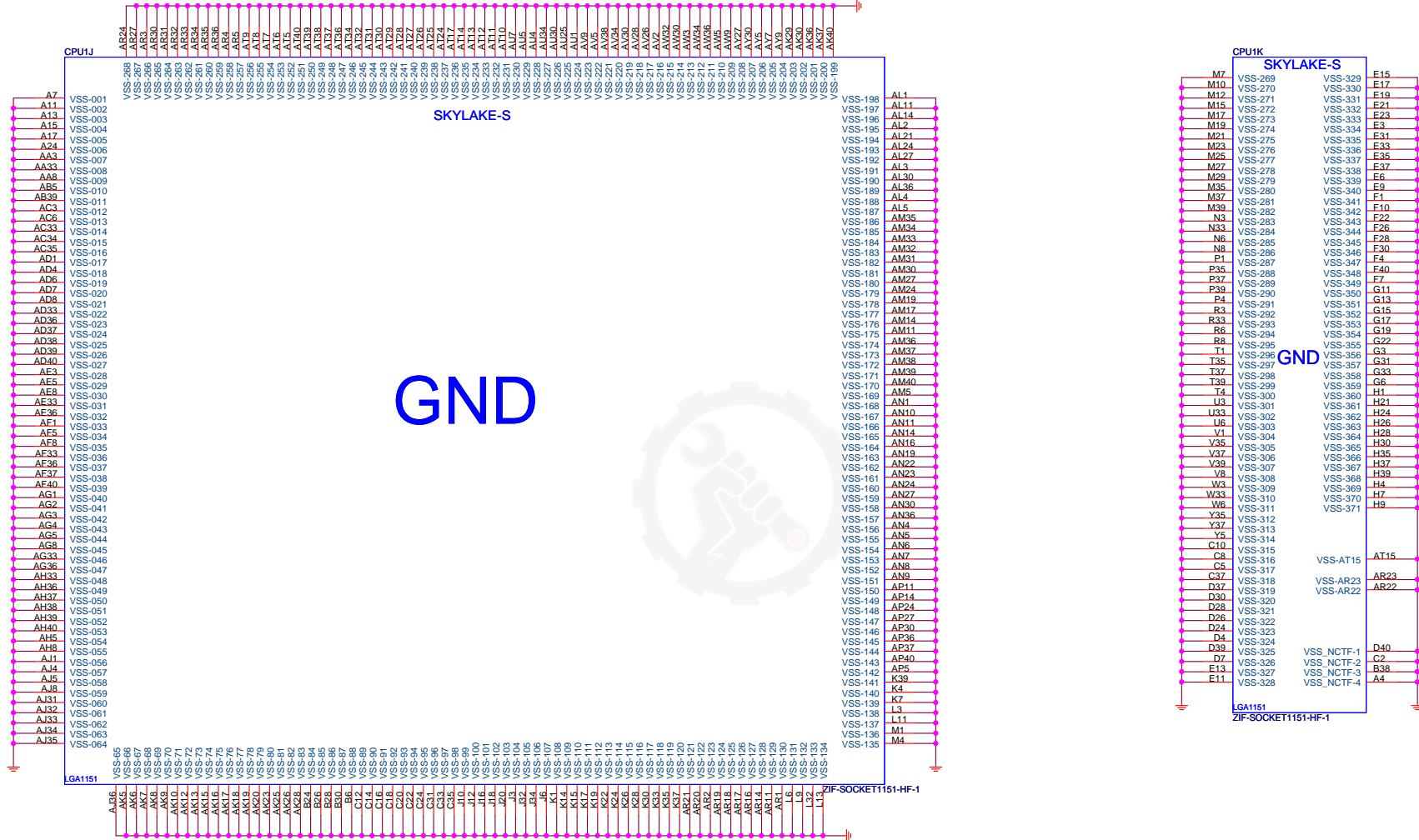
MS-7A15

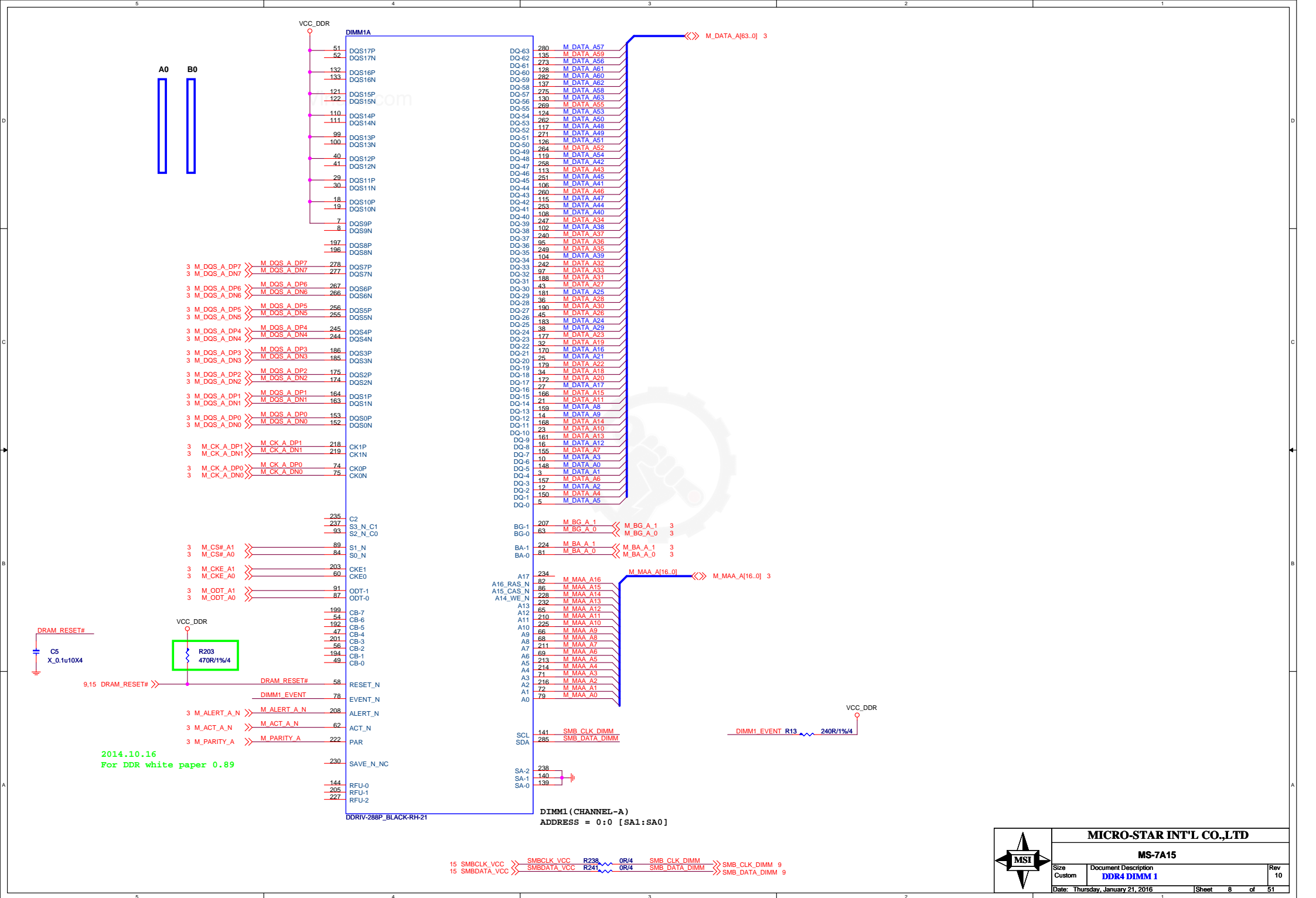
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| Size | Document Description |
| Custom | CPU-Memory |

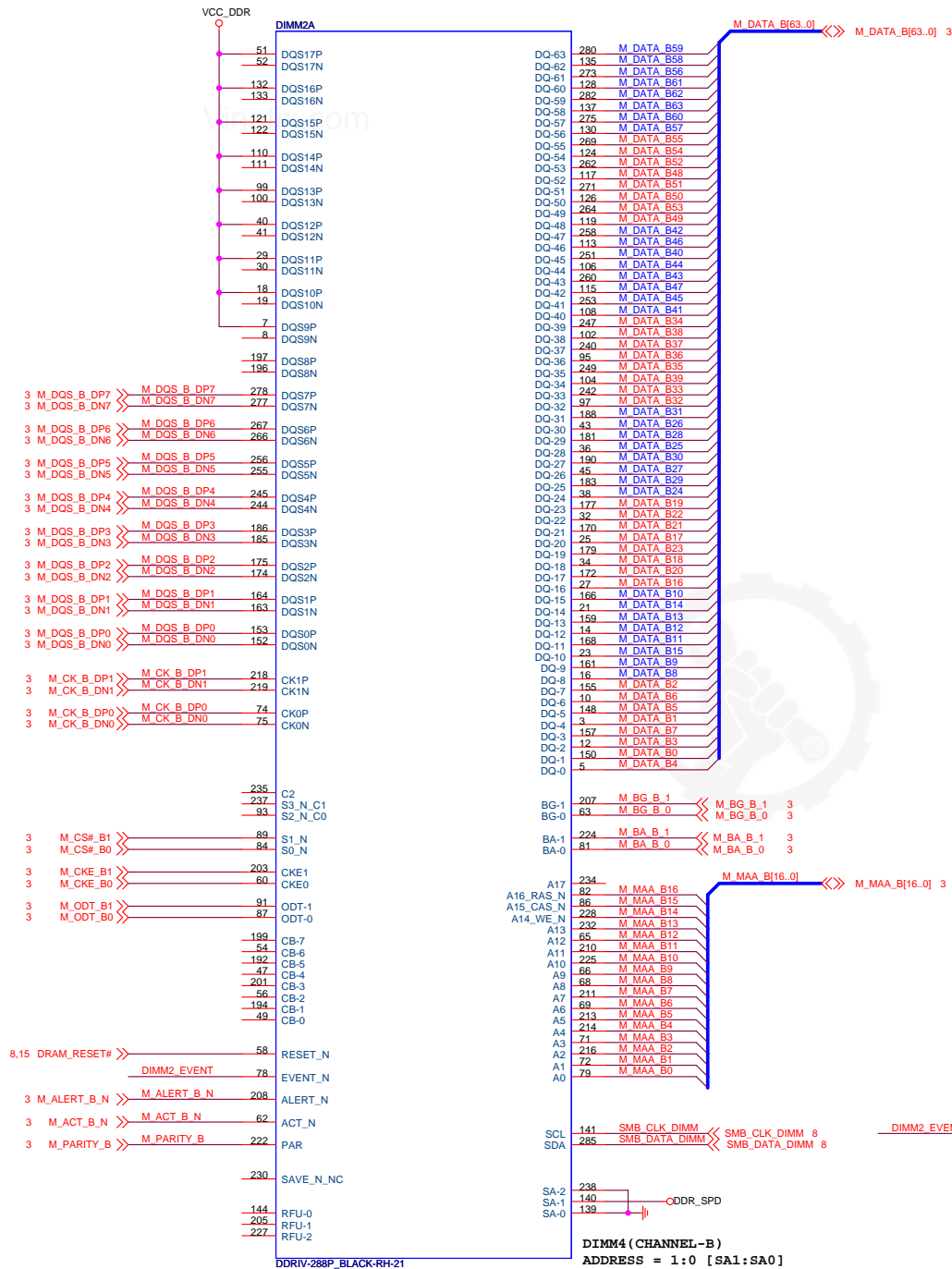
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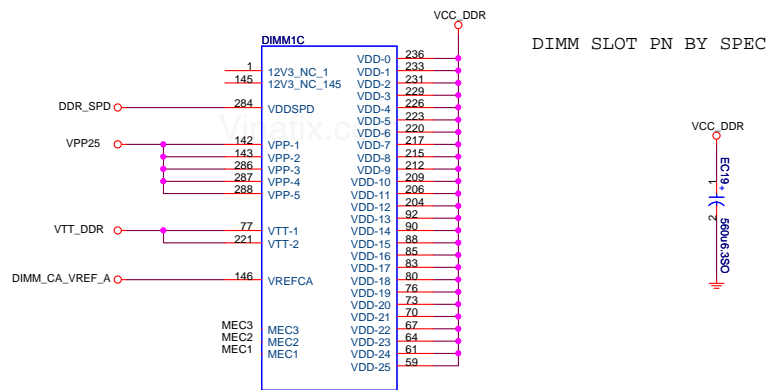




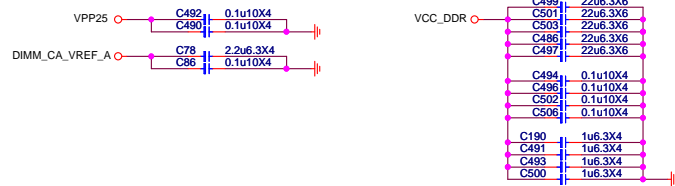
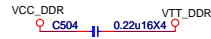




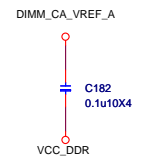
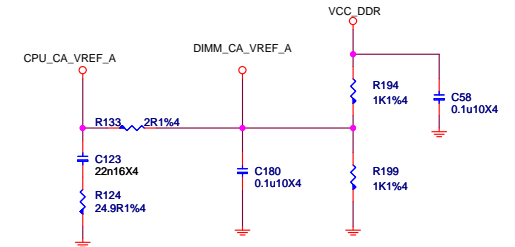
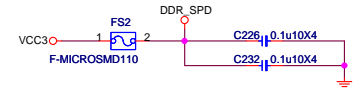
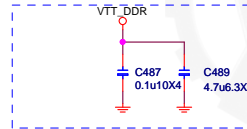
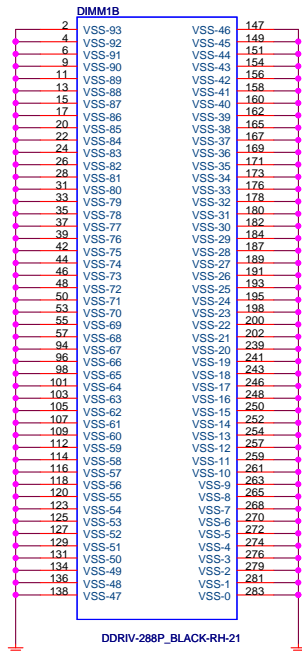
| MICRO-STAR INT'L CO.,LTD | | |
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| Size | Document Description | Rev |
| Custom | DDR4 DIMM 2 | 10 |
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DIMM SLOT PN BY SPEC



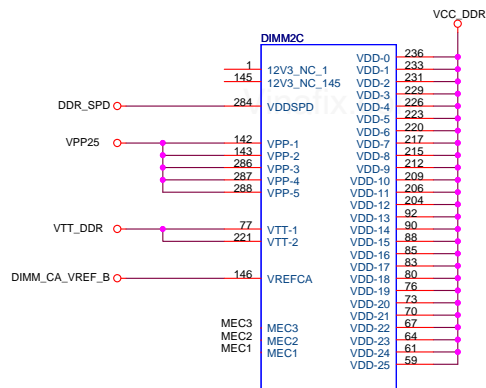
0.1uFxl per dimm



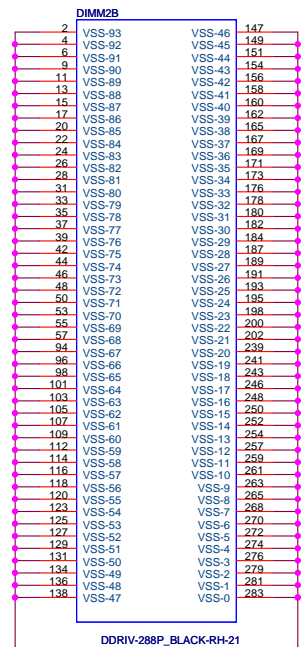
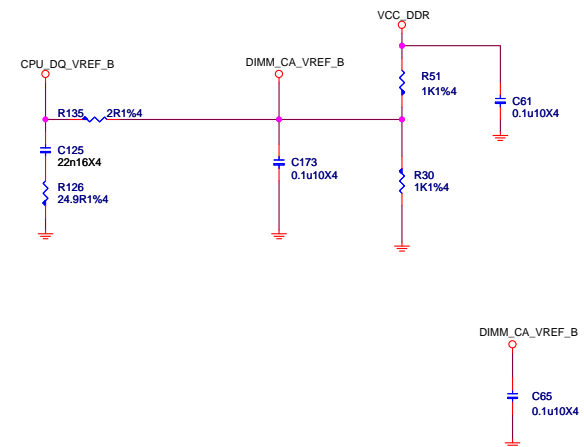
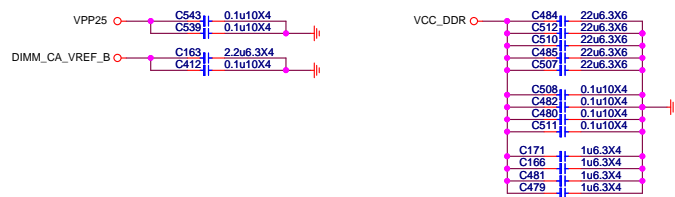
MICRO-STAR INT'L CO.,LTD

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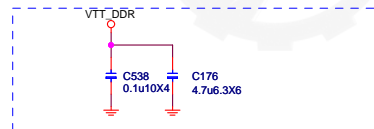
| Size | Document Description | Rev |
|----------------------------------|----------------------|-----|
| Custom | DDR4-POWER/GND-1 | 10 |
| Date: Thursday, January 21, 2016 | Sheet 10 of 51 | |

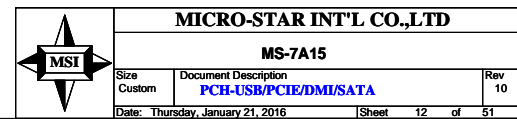


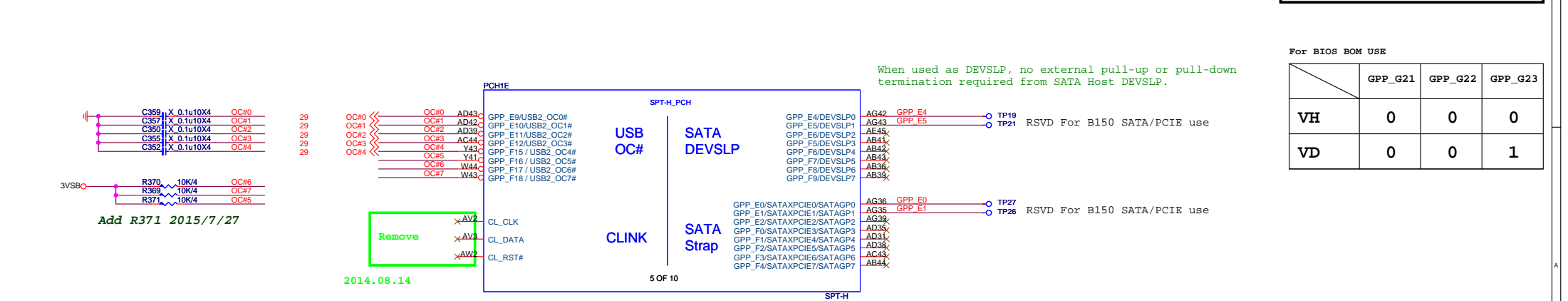
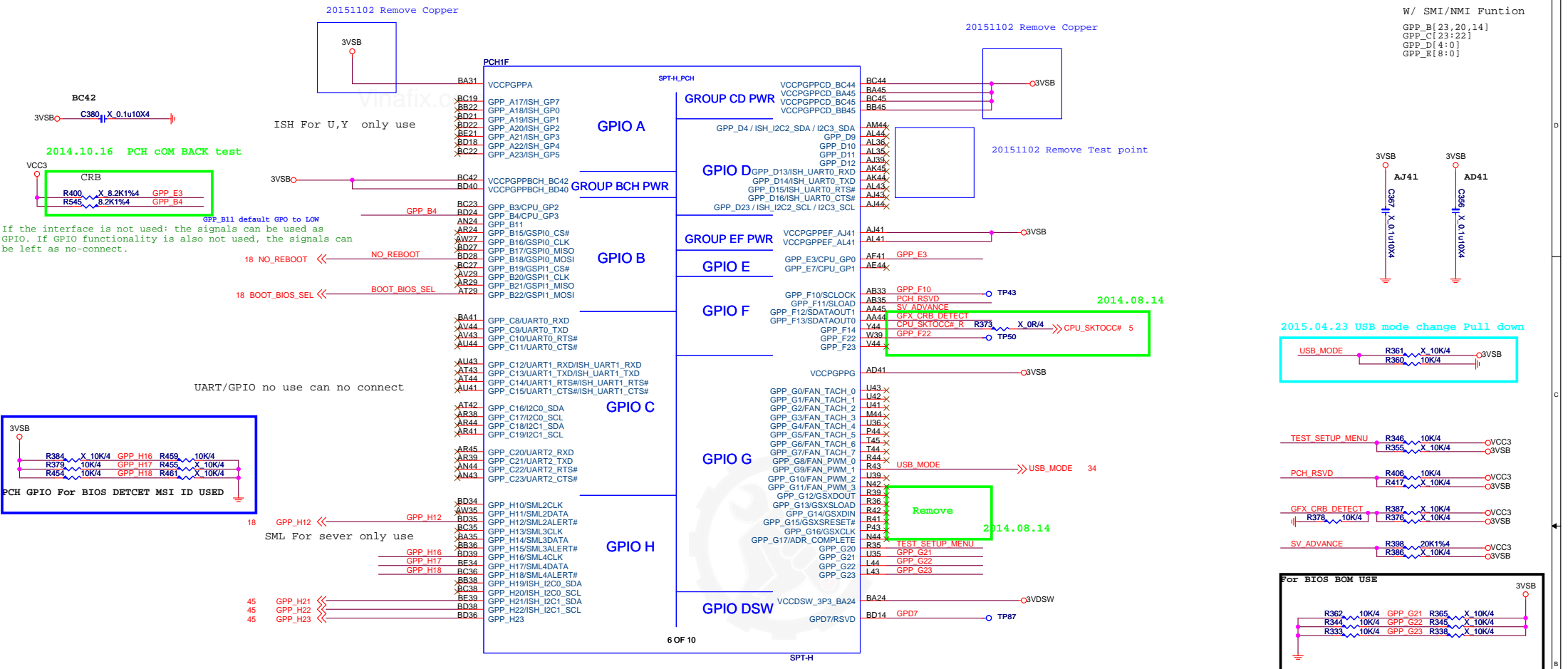
Place close to DIMM2

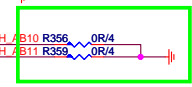
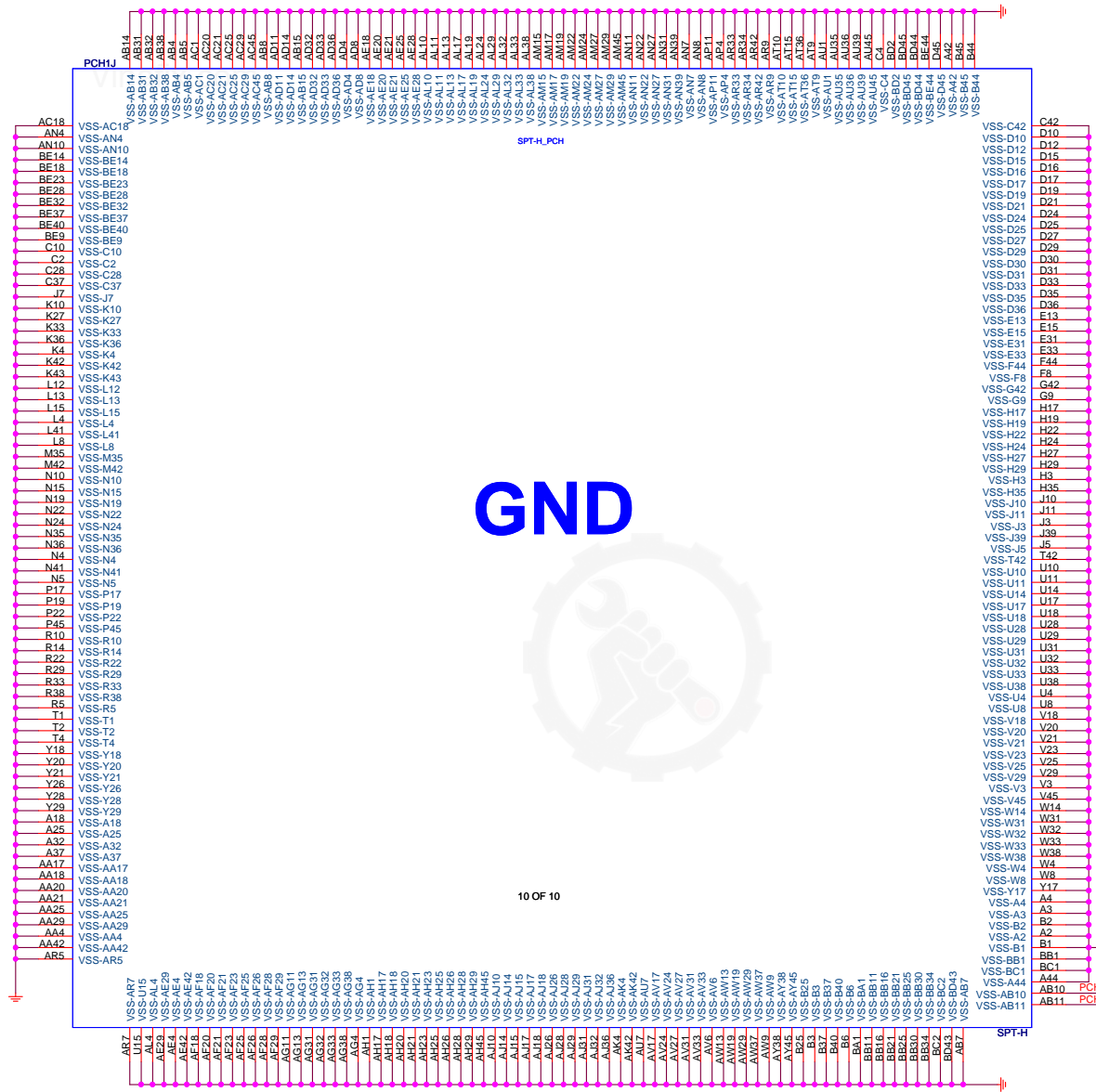


0.1uFxl per dimm



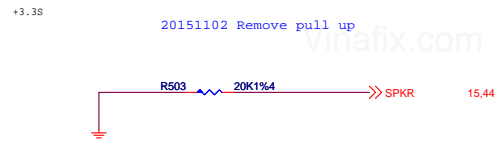






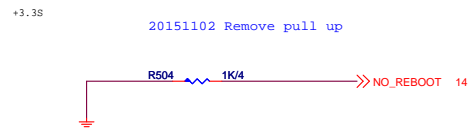
CRB 1.0 update
R356,R359 stuff
2014.09.24

TOP Swap



Internal pull-down 20K is disabled after PLTRST#

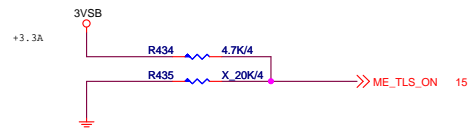
No Reboot



0 : DISABLE (Default)
1 : ENABLE

Internal pull-down 20K is disabled after PLTRST#

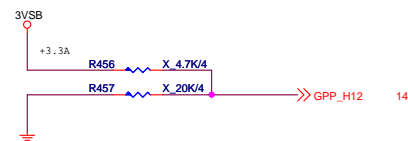
AMT and SBA with confidentiality



0 : DISABLE
1 : ENABLE (Default)

Internal pull-down 20K is disabled after RSMRST

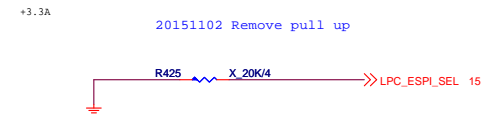
ESPI FLASH SHARING MODE



0 : MASTER ATTACHED FLASH SHARING
1 : SLAVE ATTACHED FLASH SHARING

Internal pull-down 20K is disabled after RSMRST

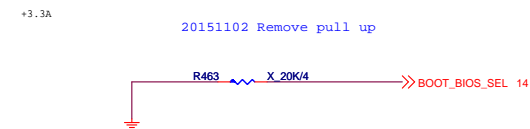
LPC eSPI Mode



0 : LPC
1 : eSPI

Internal pull-down 20K is disabled after RSMRST

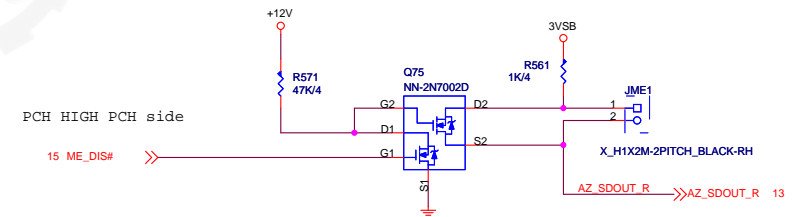
Boot BIOS

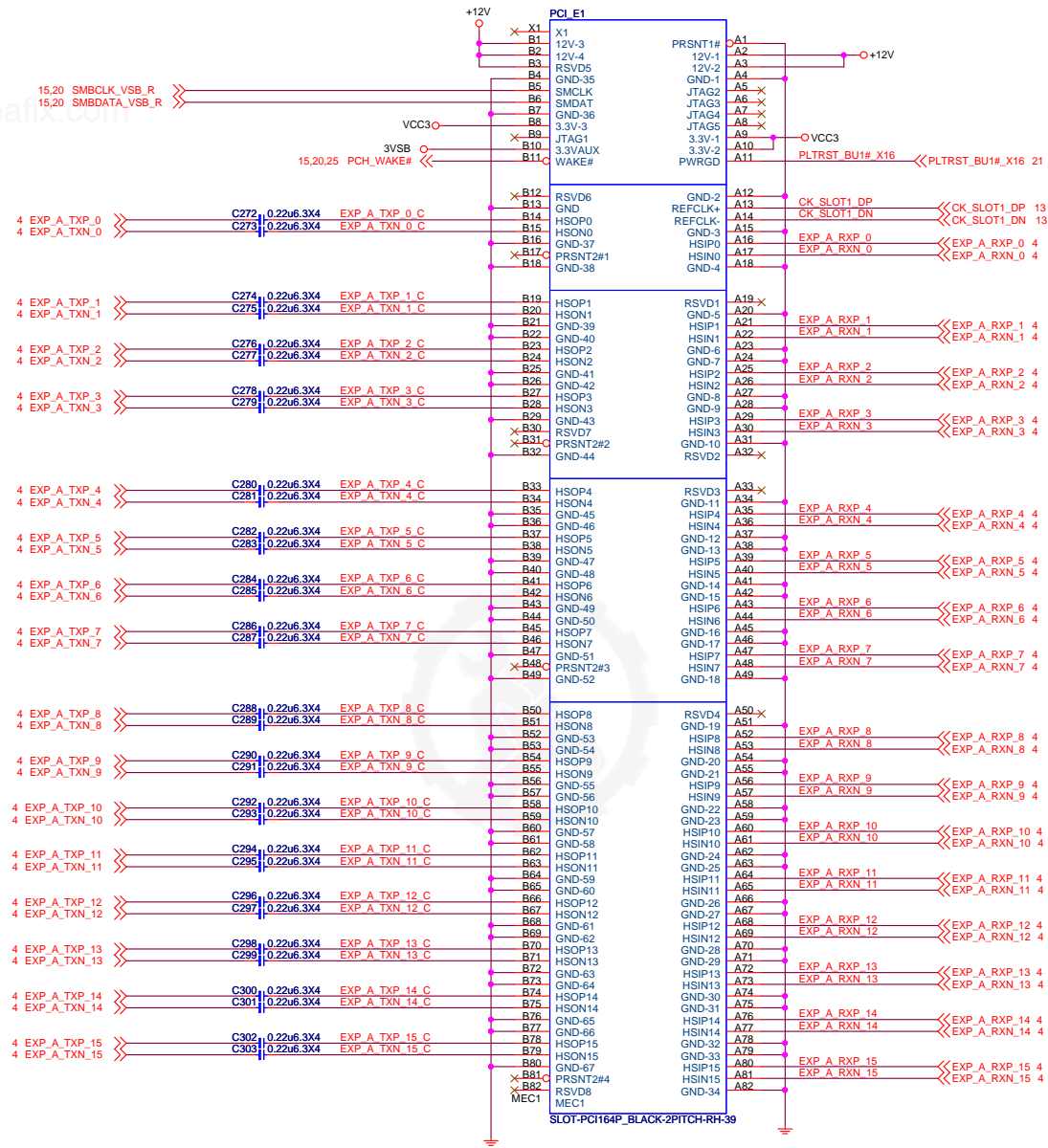
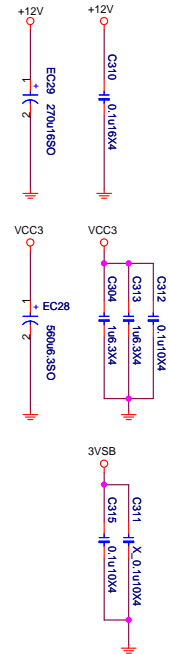


0 : SPI
1 : LPC

Internal pull-down 20K is disabled after PLTRST

HDA_SDO

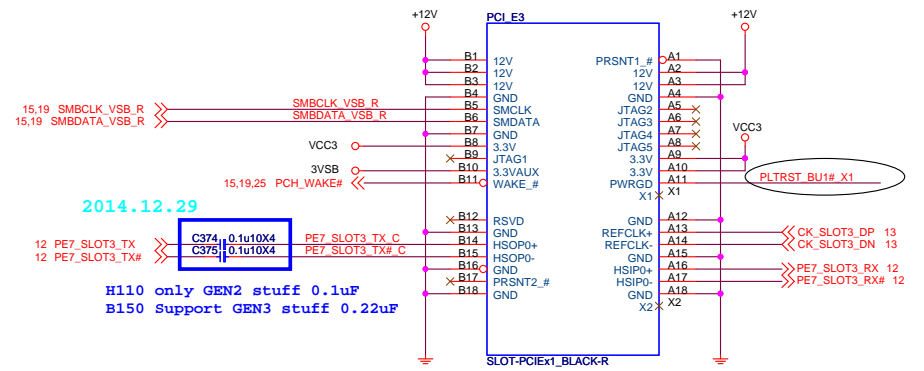
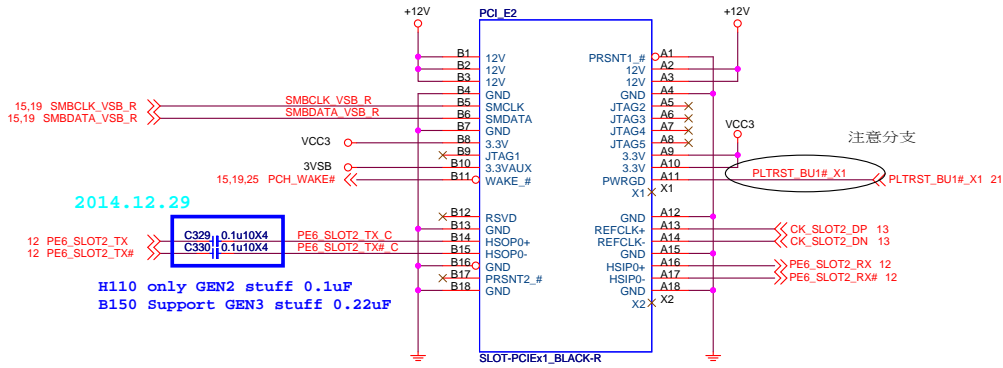




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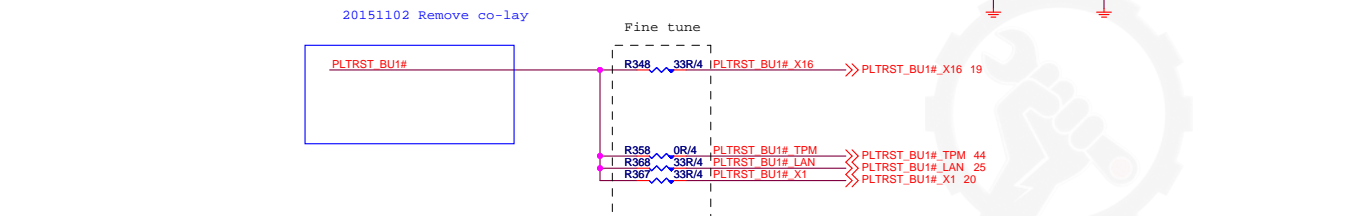
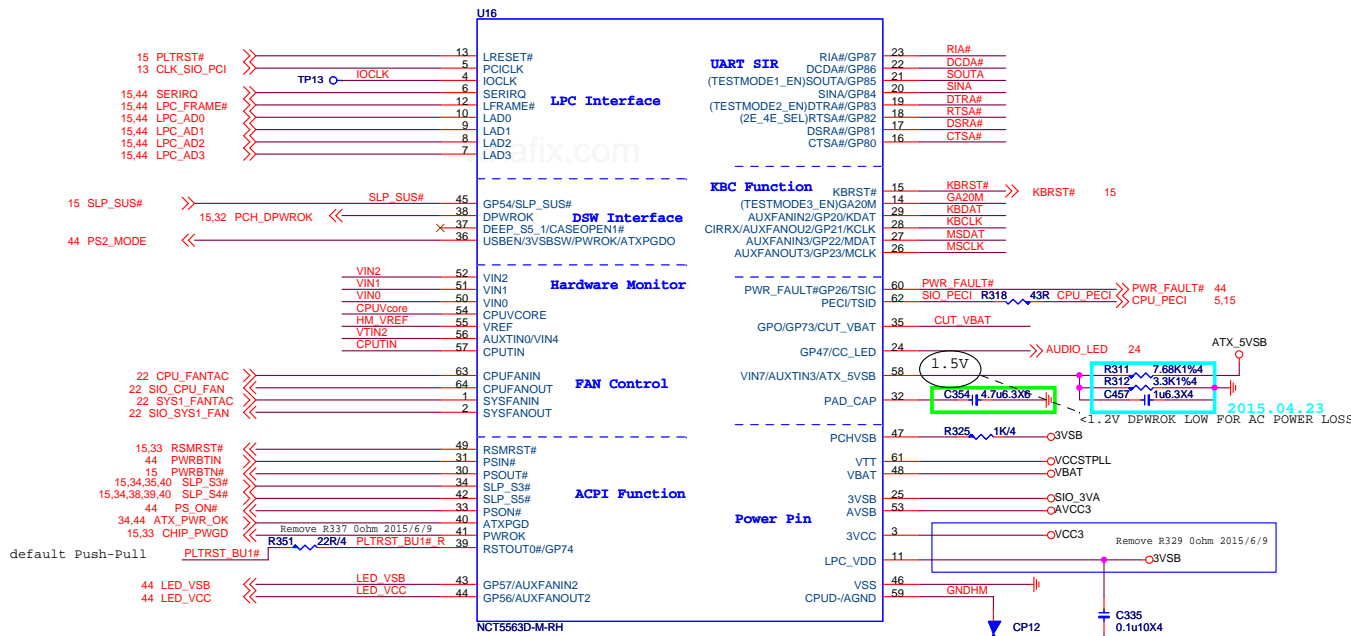
| Size | Document Description | Rev |
|--------|----------------------------|----------------|
| Custom | PCI SLOT-CPU(X16) | 10 |
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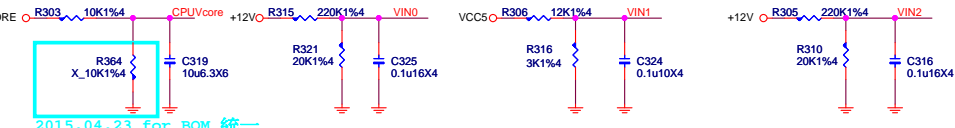
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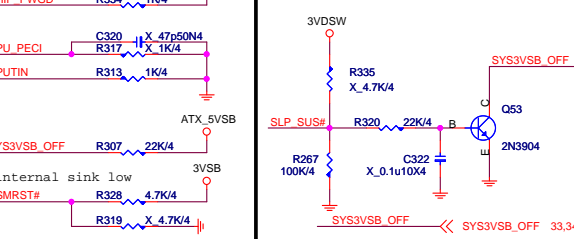
| Size | Document Description | Rev |
|--------|----------------------------|----------------|
| Custom | PCIE SLOT-PCH(X1) | 10 |
| Date: | Thursday, January 21, 2016 | Sheet 20 of 51 |



HW Monitor - Voltage



5563D DSW SUPPORT



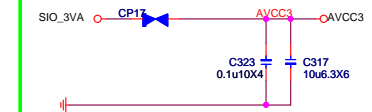
Thermal Monitor



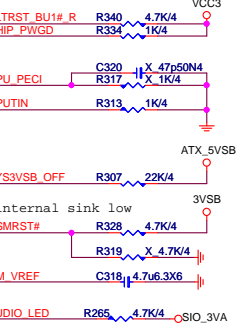
| | R350 | R329 | R357 | R309 | C354 |
|-------|------|------|------|------|------|
| 5562D | O | X | O | O | X |
| 5563D | O | O | O | O | O |

20151102 Remove co-lay power

3V Analog Power

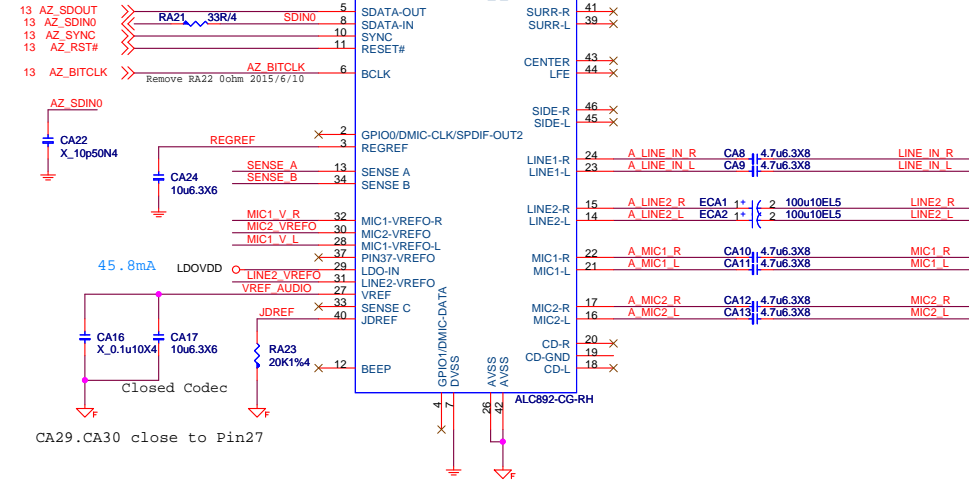


default Push-Pull

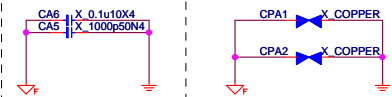


Type B: ALC892/887

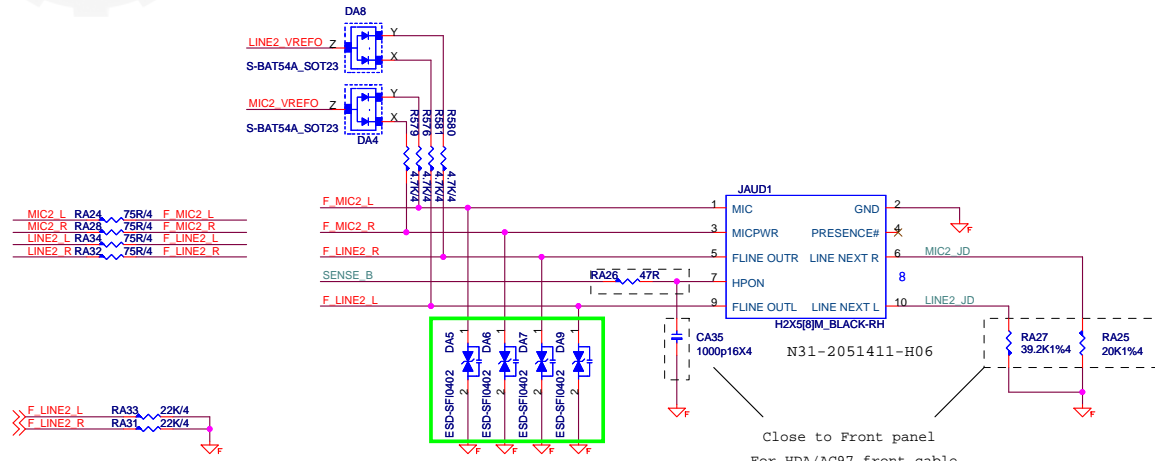
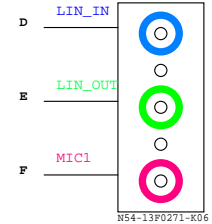
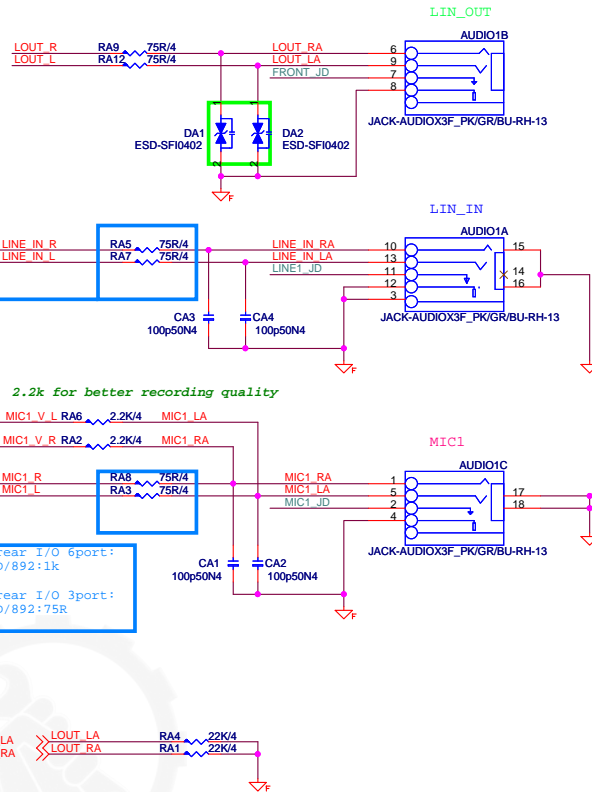
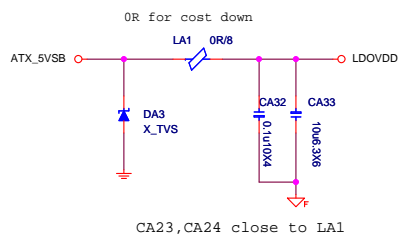
Closed code 2015/6/22



EMI



Closed Codec

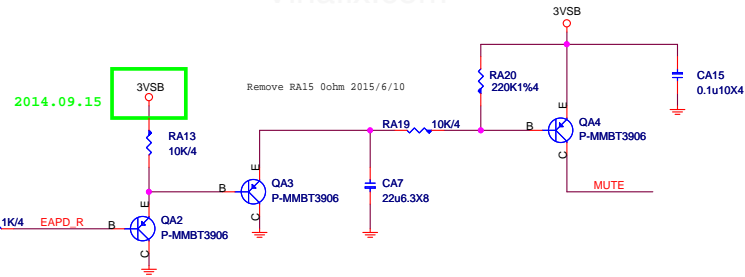


Varistor --> cap for cost down
D0G-2950500-SI0
D0G-3010510-I05
Close to Jack

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| MS-7A15.. | | | |
| Size | Document Description | Rev | |
| Custom | AUDIO - ALC892/887 | 10 | |
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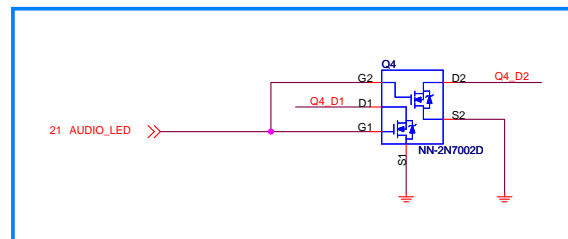
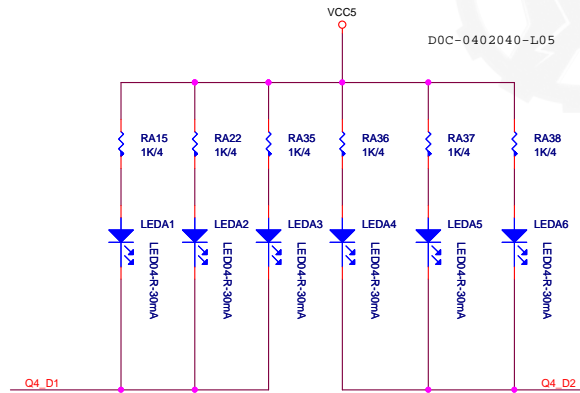
Rear Line OUT De-POP circuit

De-pop circuit for Rear Line out & Front Headphone out)



Digital

Analog



2016.01.12:Modify Q4 to Dual 7002 & Remove OR

History:

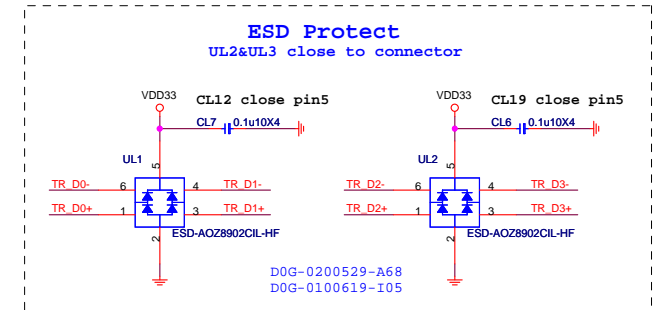
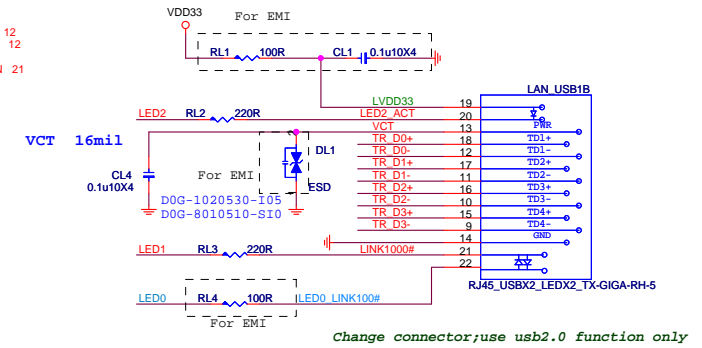
2014/02/13: stuff de-pop circuit of Line out & HP out.

RTL8111G/RTL8111H Giga LAN

8111H:B06-08111CC-R09
8111G:B06-081116C-R09

Vinafix.com

LAN Connector



Pin33: 4 via from top layer to GND layer
and make the via at the center of IC.

8111G POWER Consumption

| | 3.3V @ mA | mW |
|-----------------|-------------|-------------|
| 10 M Idle/TxRx | 17.15/116.7 | 56.6/385.1 |
| 100 M Idle/TxRx | 71.45/129.5 | 235.8/427.4 |
| Giga Idle/TxRx | 179.1/243.9 | 591/804.9 |
| ALDPS | 6.41 | 21.15 |

8111H POWER Consumption

| | 3.3V @ mA | mW |
|-----------------|--------------|---------------|
| 10 M Idle/TxRx | 9.9/84.69 | 32.67/279.48 |
| 100 M Idle/TxRx | 48.11/92.44 | 158.76/305.05 |
| Giga Idle/TxRx | 124.5/177.57 | 410.85/585.98 |
| ALDPS | 5.50 | 18.15 |

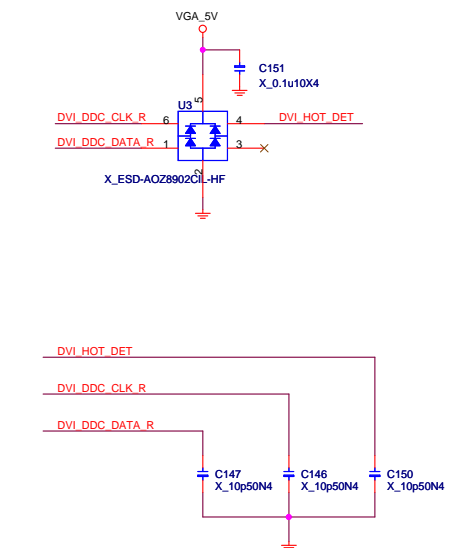
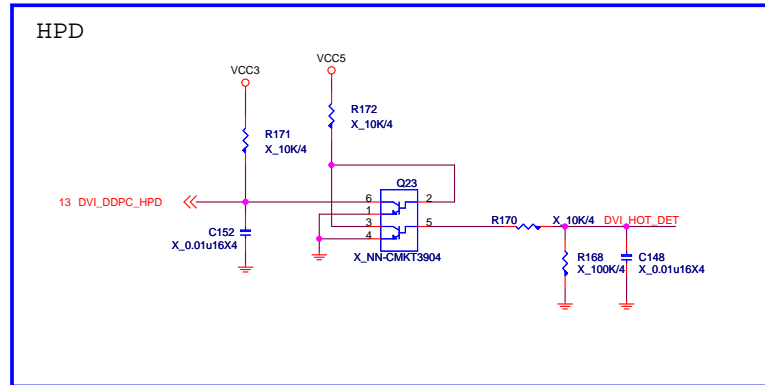


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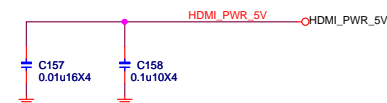
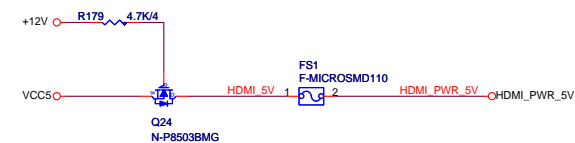
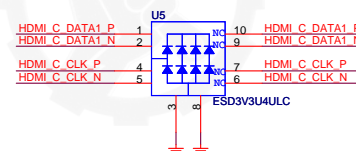
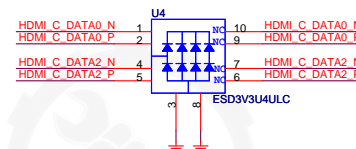
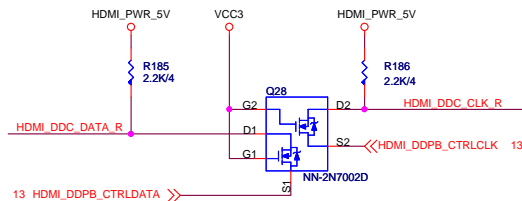
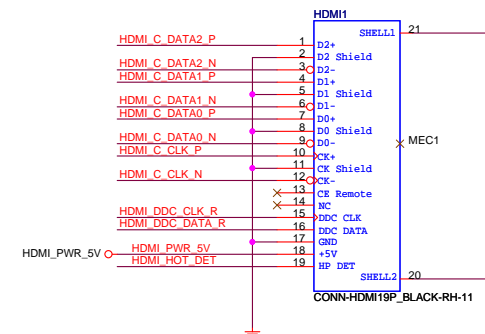
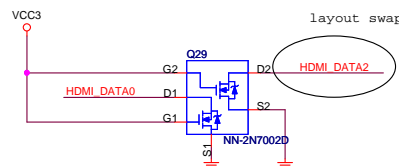
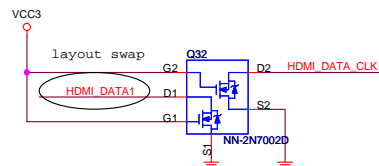
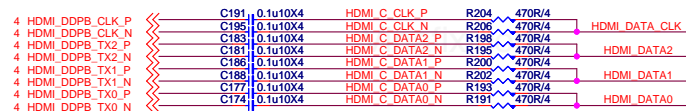
| Size | Document Description | Rev |
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| Custom | LAN - RTL8111H | 10 |
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VGA: resolution of 2048x1536 pixels with 32-bit color at 75 Hz (4:3 QXGA)

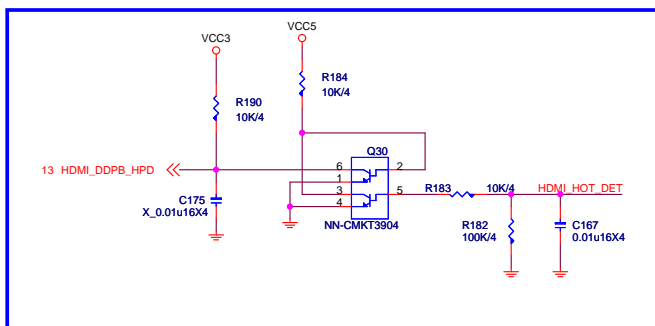
**MS-7A15**

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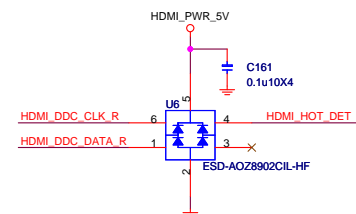
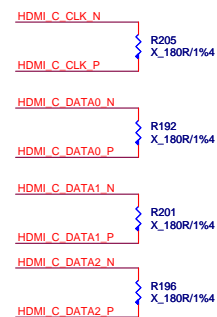
HDMI, DVI : 1920x1200 at 60 Hz (16:10 WUXGA)



HPD

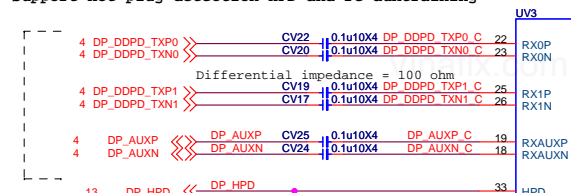


For EMI



Note:

If connect to eDP port, must confirm whether it support hot plug detection HPD and re-auxtraining

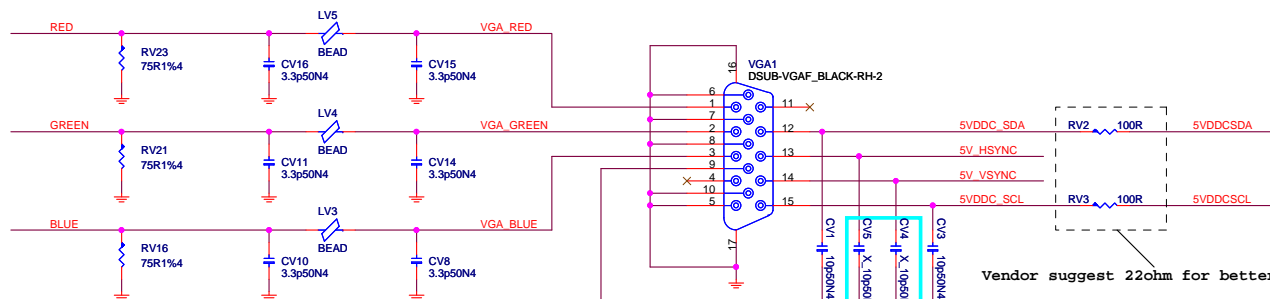
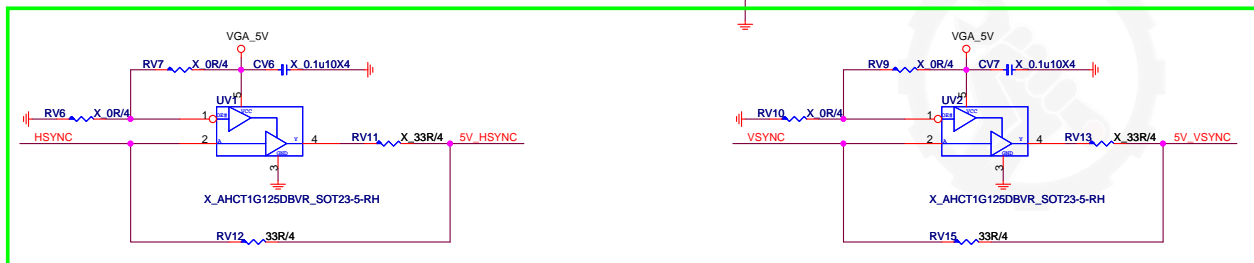


IT6515FN

Add 0ohm R103
2015/09/10

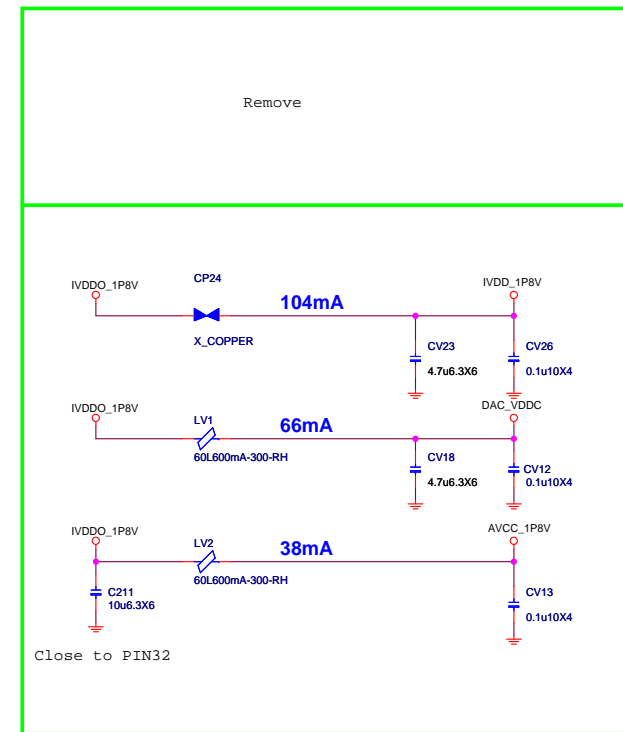
close to PIN 29

260mA



Vendor suggest 22ohm for better I2C quality

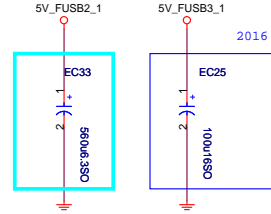
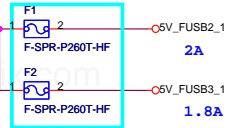
2015.01.09
For SA test fail



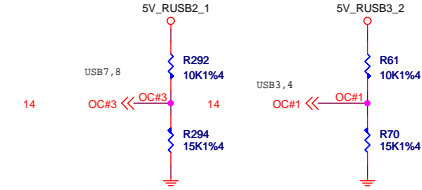
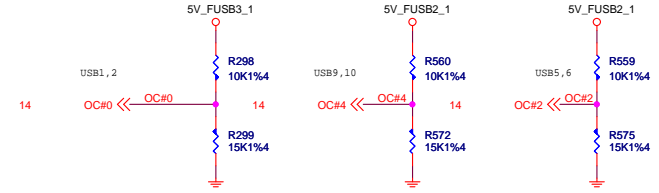
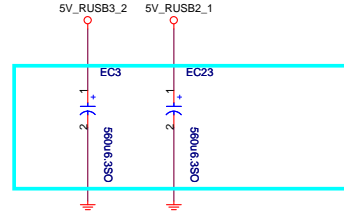
| MICRO-STAR INT'L CO.,LTD | | | |
|----------------------------------|----------------------|-----|-------|
| MS-7A15 | | | |
| Size | Document Description | Rev | |
| Custom | VGA - ITE6515 | 10 | |
| Date: Thursday, January 21, 2016 | Sheet | 28 | of 51 |

20151105 Modify to 5VDIMM

20150317 change to IVY mail

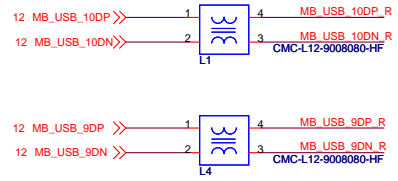


20150924 change USB CAP

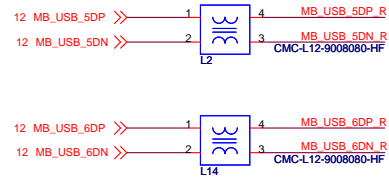


Remove OC#5 2015/07/27

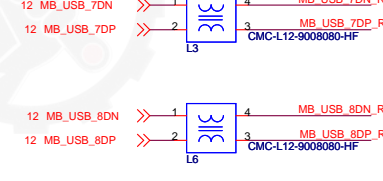
FRONT USB PORT 9,10



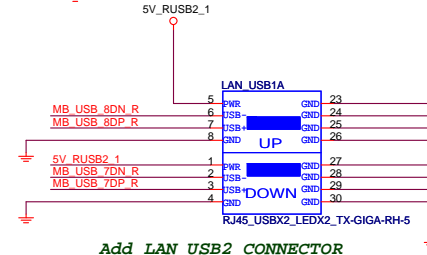
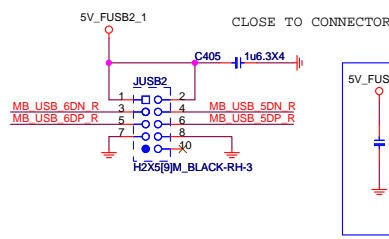
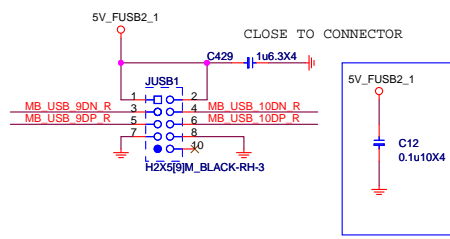
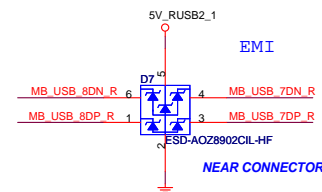
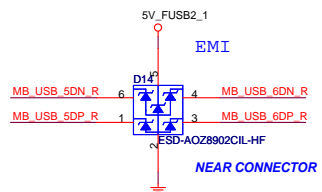
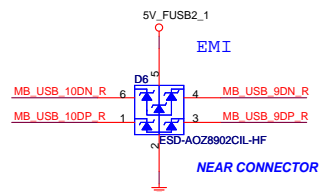
FRONT USB PORT 5,6



REAR USB PORT 7,8

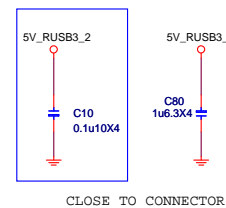
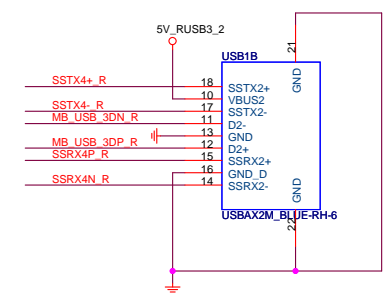
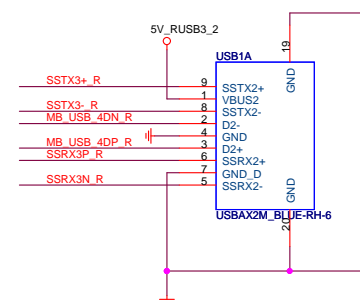
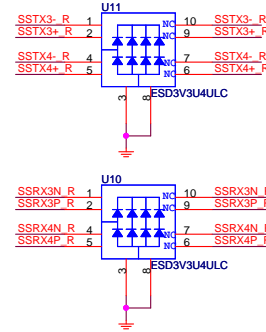
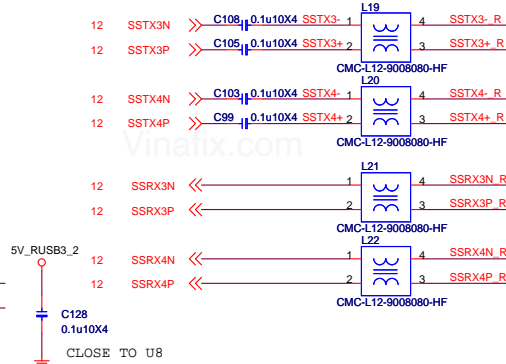
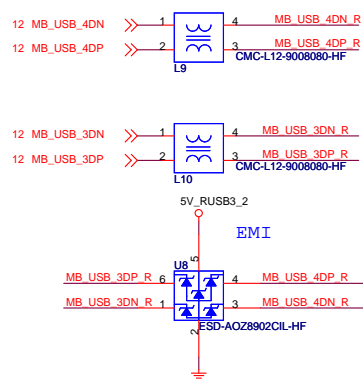


Remove Port 11 12
2015/27/27

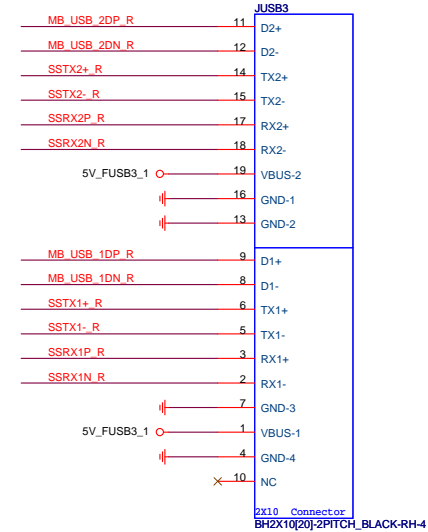
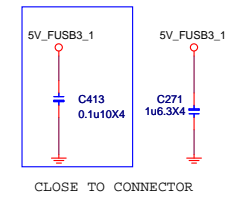
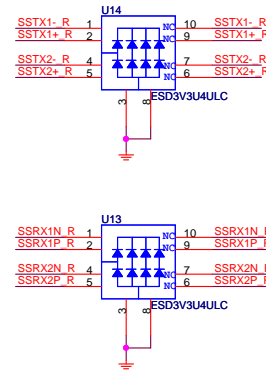
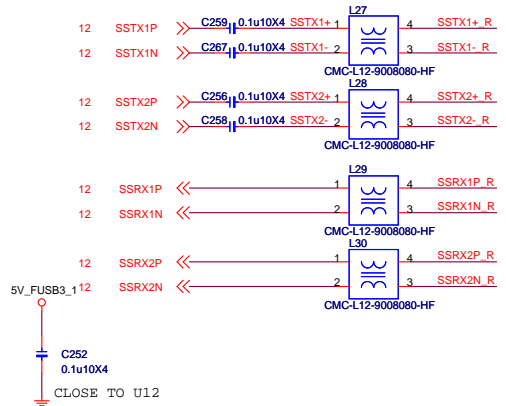
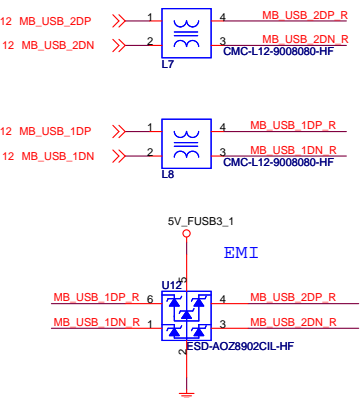


| MICRO-STAR INT'L CO.,LTD | | |
|--------------------------|----------------------------|----------------|
| MS-7A15 | | |
| Size | Document Description | Rev |
| Custom | USB2.0 Connector | 10 |
| Date: | Thursday, January 21, 2016 | Sheet 29 of 51 |

Add LAN USB2 CONNECTOR
2015/7/27

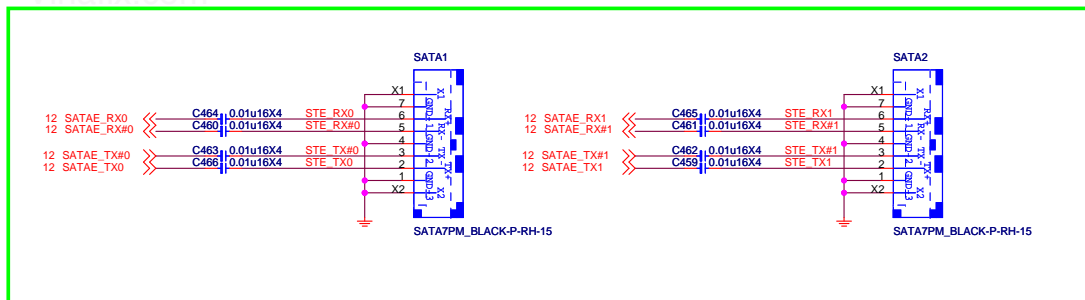


Remove LAN USB3 function
(PORT5/6)
2015/7/27

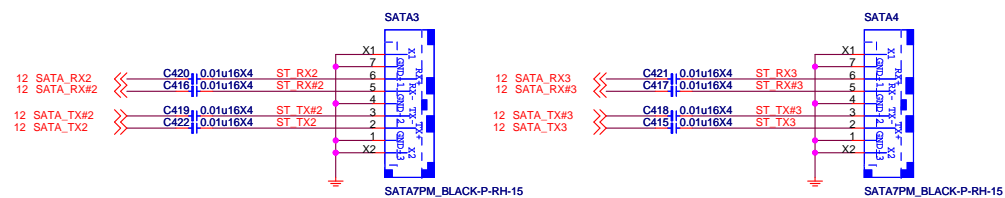


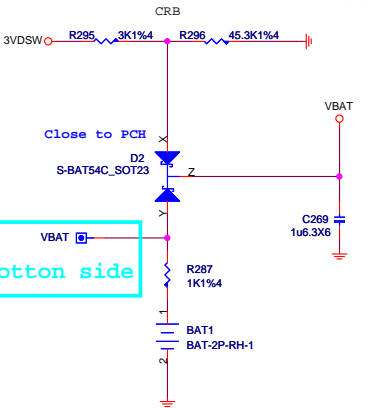
| | | | |
|--------------------------|-----------------------------|-------|----------|
| | | | |
| MICRO-STAR INT'L CO.,LTD | | | |
| MS-7A15 | | | |
| Size | Document Description | Rev | |
| Custom | Rear USB3 & Front Connector | 10 | |
| Date: | Thursday, January 21, 2016 | Sheet | 30 of 51 |

SATAE change to SATA PORT0 PORT1 2015.05.28

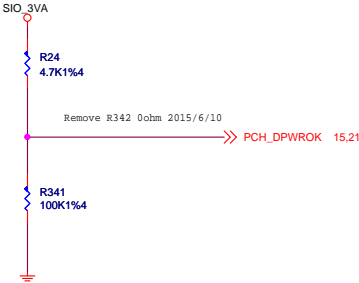


Remove 90 angle SATA connector
2015/7/27

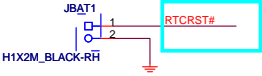




RTCRST# 15,34

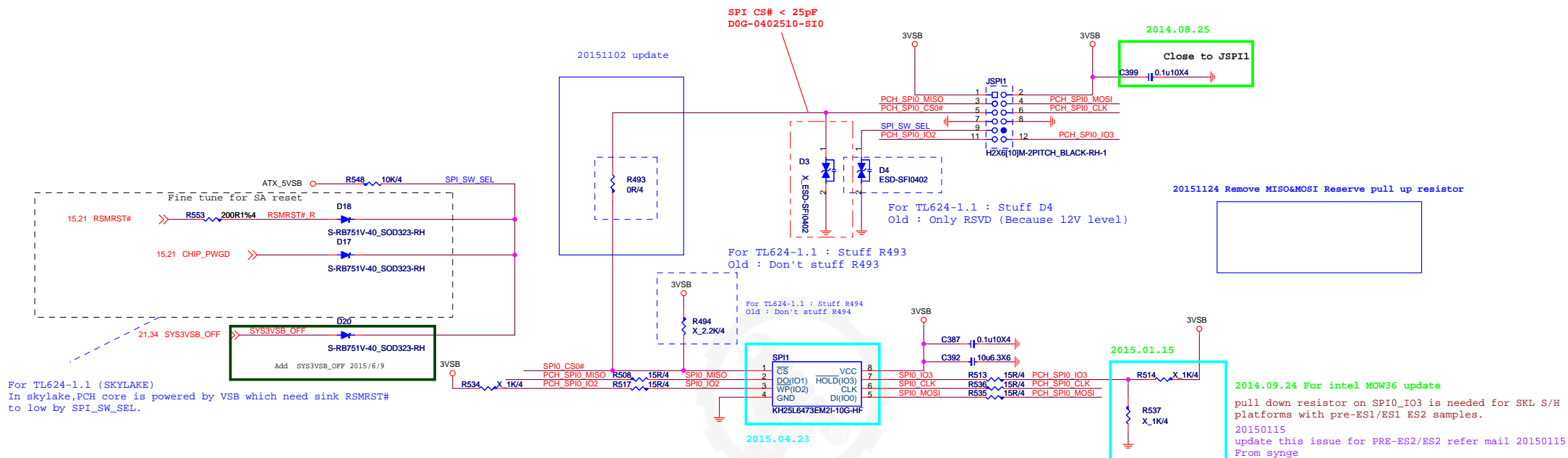


2016.01.13:Remove R587&C433,PCH Have Pull up to VBAT



15 PCH_SPI0_MOSI << PCH_SPI0_MOSI
15 PCH_SPI0_MISO << PCH_SPI0_MISO
15 PCH_SPI0_CLK << PCH_SPI0_CLK
15 PCH_SPI0_CS0# << PCH_SPI0_CS0#
15 PCH_SPI0_IO2 << PCH_SPI0_IO2
15 PCH_SPI0_IO3 << PCH_SPI0_IO3

Vinafix.com



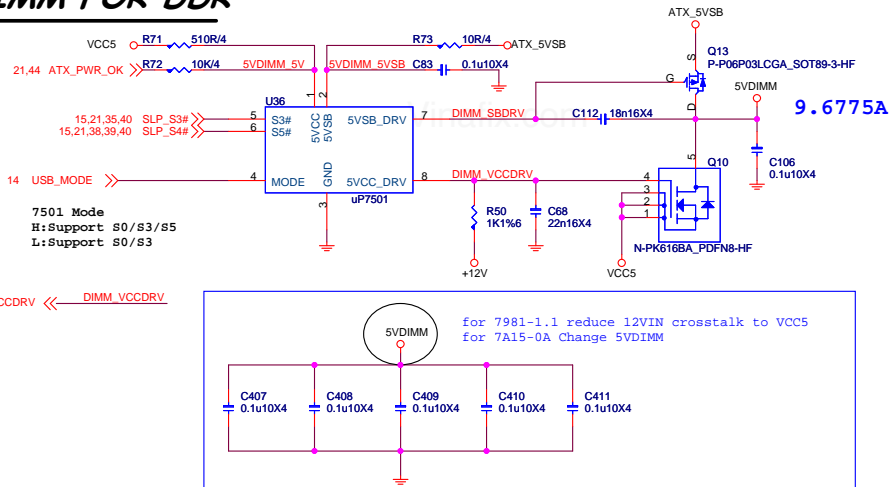
- * if you not support Standby power in S5 Status, component Q14.G Pull-high to +12V & Q14 MOS select 2N7002
 - * if you support Standby power in S5 Status(Ex: PCH is B75 Chipset) , component Q14.G Pull-high to ATX_5VSB , Q14 must select "Vth" under 1V (Component Suggestion as below)
- D03-0341409-A68 / D03-0230019-A30



| MICRO-STAR INT'L CO.,LTD | | |
|----------------------------------|----------------------------------|-----------|
| MS-7A15 | | |
| Size Custom | Document Description BIOS ROM | Rev 10 |
| Date: Thursday, January 21, 2016 | Sheet 33 of 51 | |

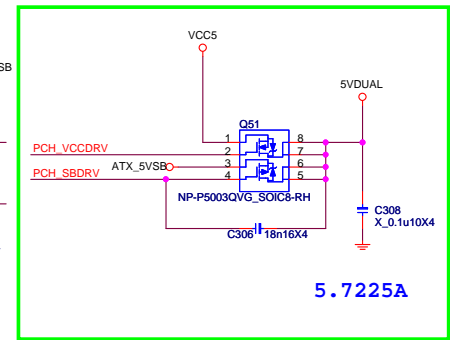
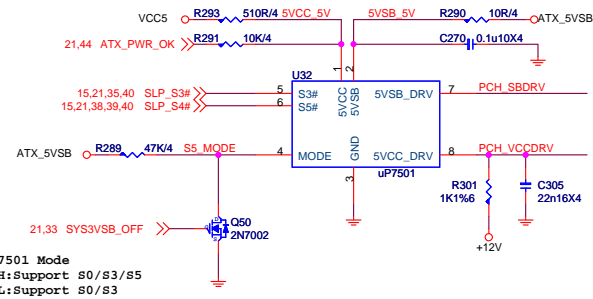
5VDIMM FOR DDR

(3A for DDR, 6.6A for USB)



5VDUAL

5VDUAL is power source of 1P0SB, 1.8PSB & 3VSB



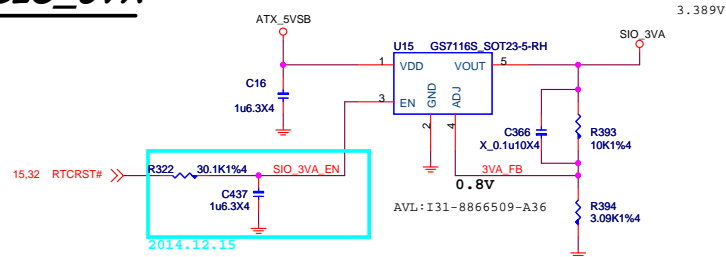
2015.09.15

For power 700W solution (only for uP7501+uP7506 for 3VSB solution)
The power supply VCC3 delay 12ms after VCC5 assert.
The chip U7501 PCH_VCCDRV work when the VCC5 ready
(When VCC5 up to 4.2V and the 5VDRV1 delay 6ms assert), but
VCC3 not ready and let the 3VSB sequence fail.

20151106 :Remove 3VSB Patch Circuit

SIO_3VA

20mA

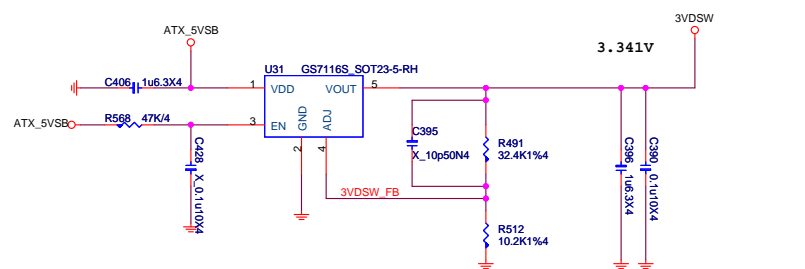


2014.12.15

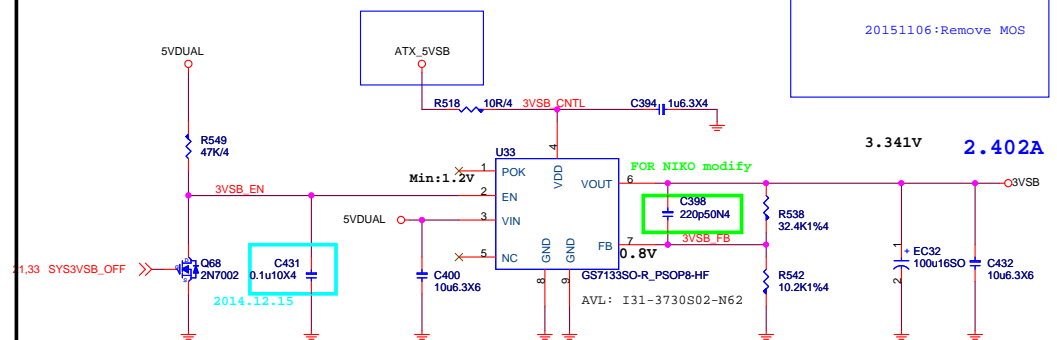
20151110 Modify to GS7116

3VDSW

204mA



3VSB cost down



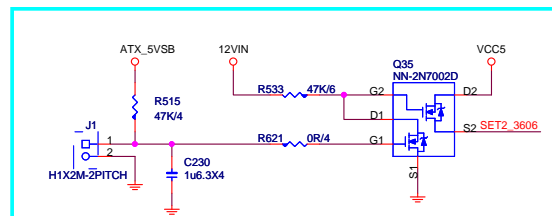
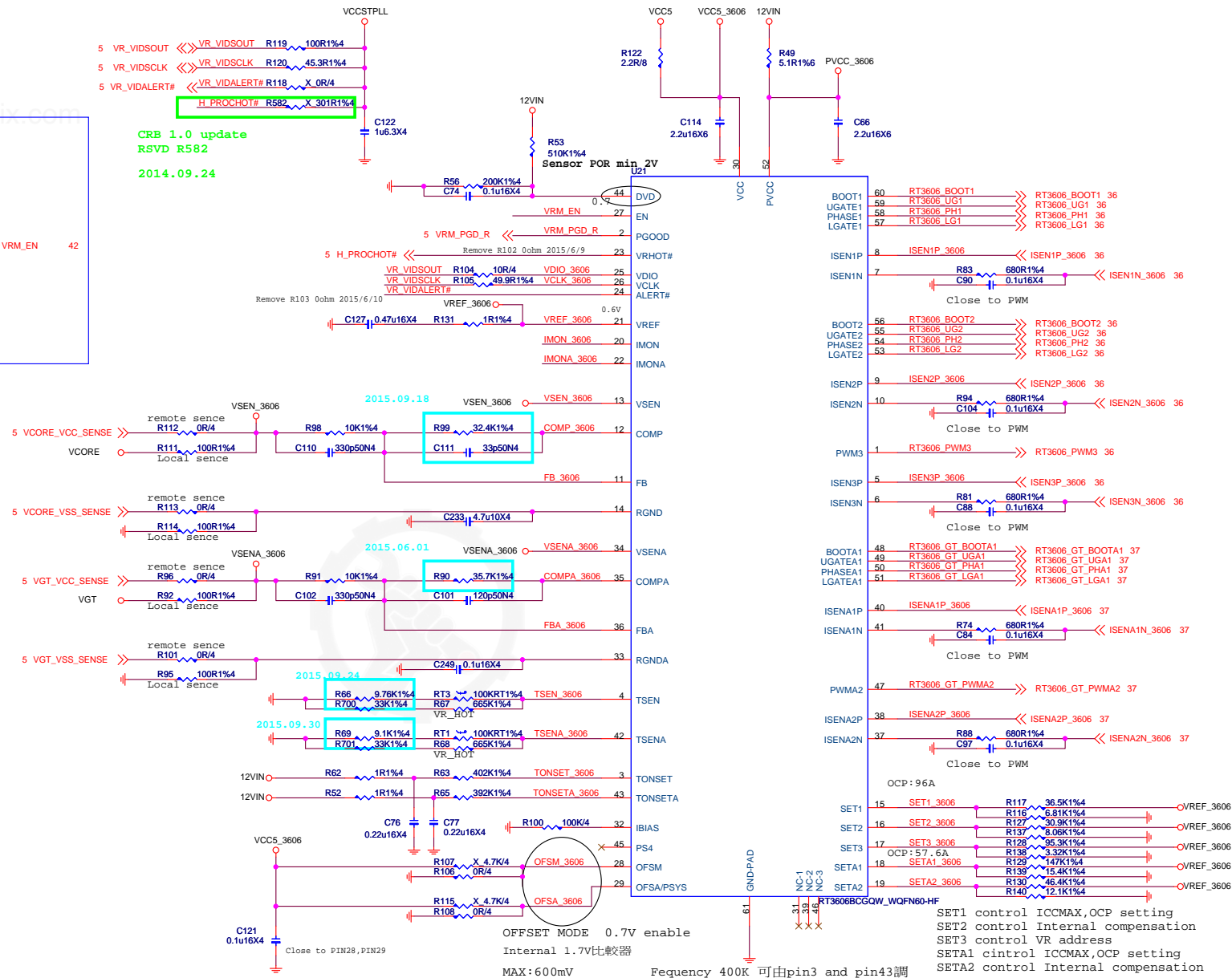
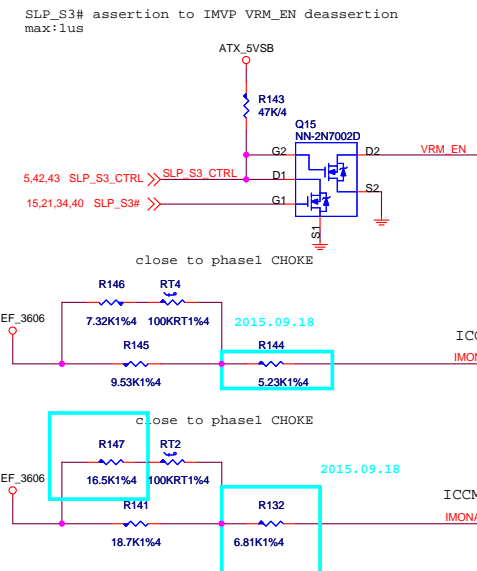
20151106:Remove MOS



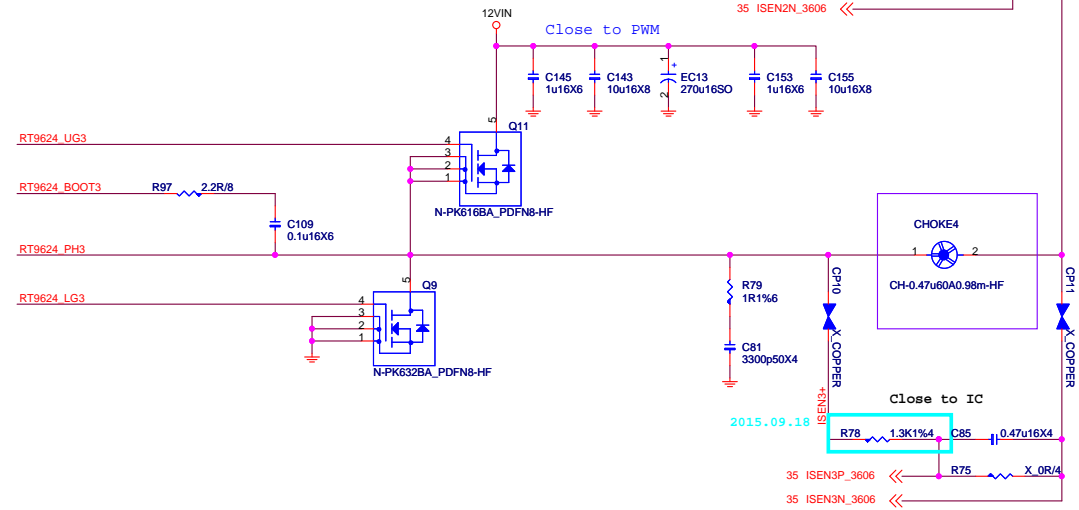
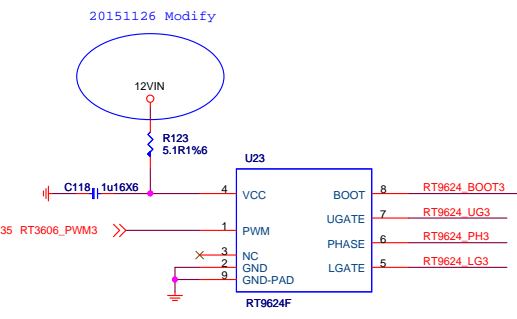
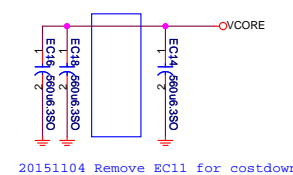
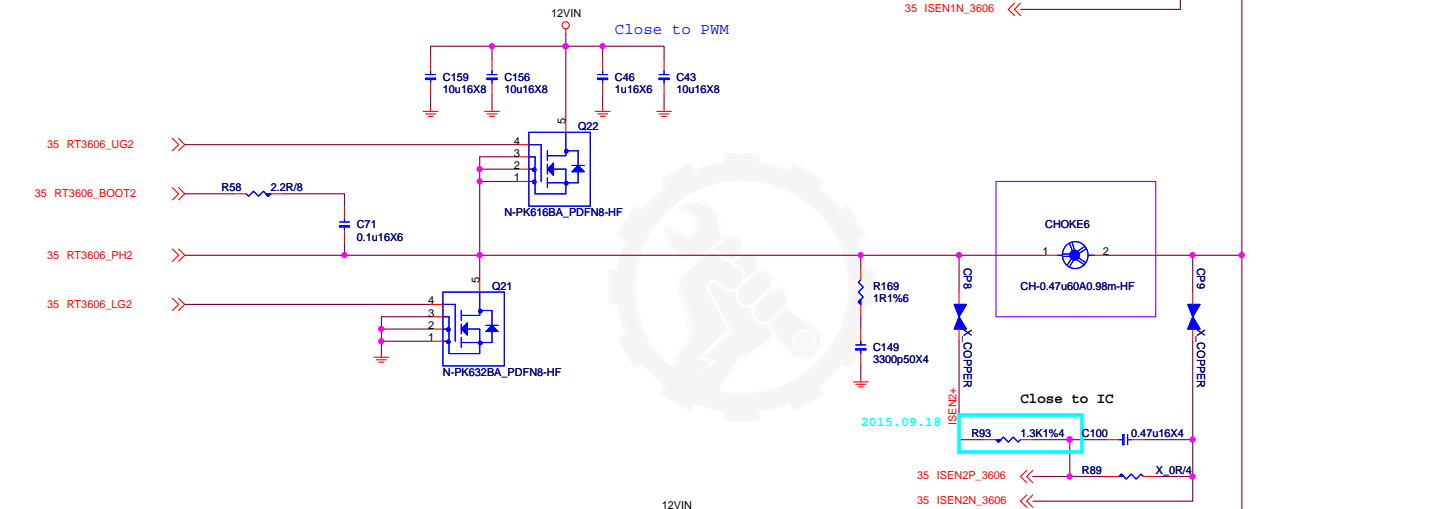
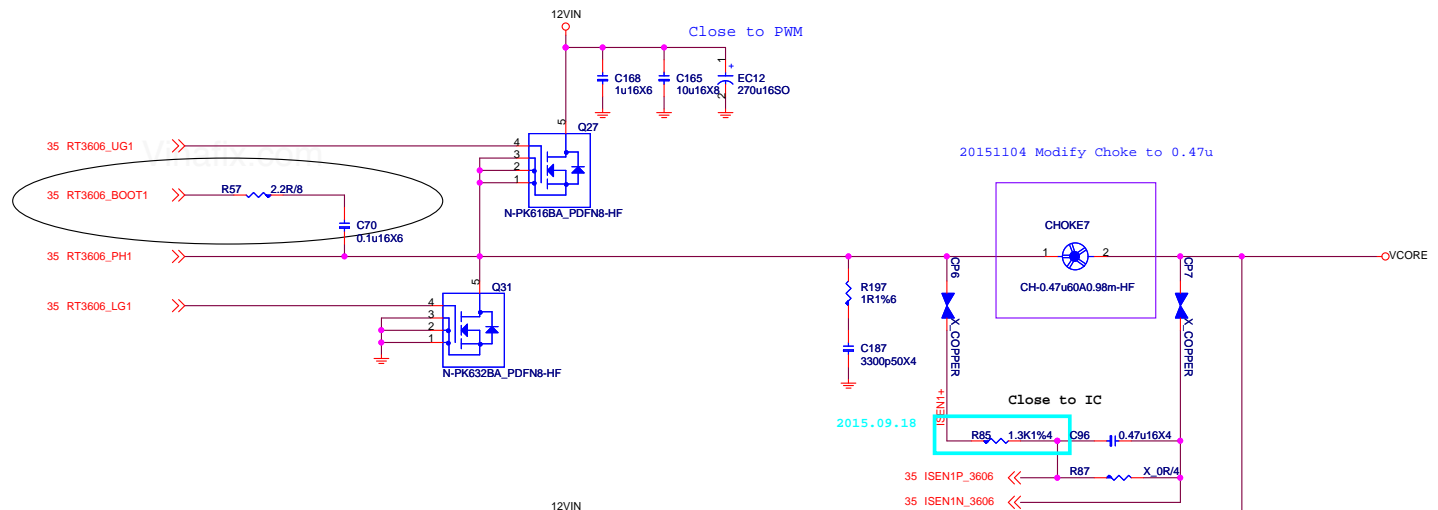
MICRO-STAR INT'L CO.,LTD

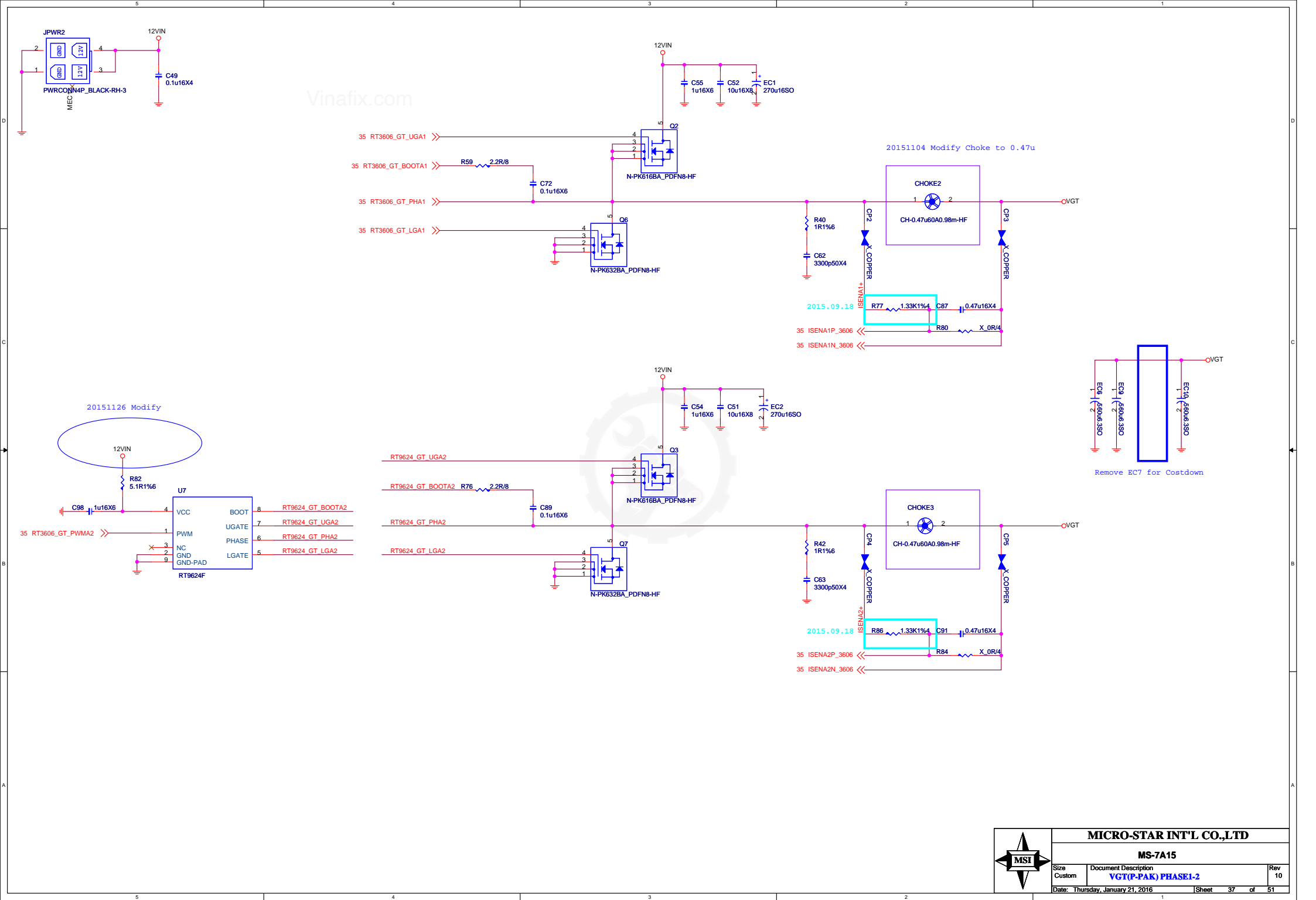
MS-7A15

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|--------|----------------------------|----------------|
| Custom | ACPI CONTROLLER | 10 |
| Date: | Thursday, January 21, 2016 | Sheet 34 of 51 |



| | | | |
|---------------------------------|---|-------|-------|
| MICRO-STAR INT'L CO.,LTD | | | |
| MS-7A15 | | | |
| Size Custom | Document Description PWM-RT3606BC | Rev 1 | |
| Date: Friday, January 22, 2016 | Sheet | 35 | of 51 |





DDR4_1.2V 2.8A+ 4.75A+0.375A=7.925

2.8A FOR CPU
4.8A FOR 2DIMM DDR3
0.375A FOR VTT_DDR

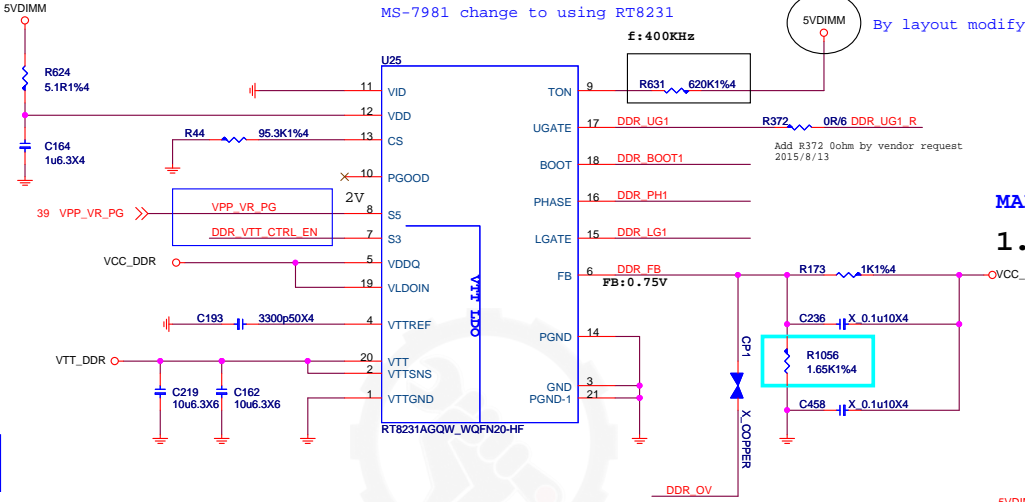
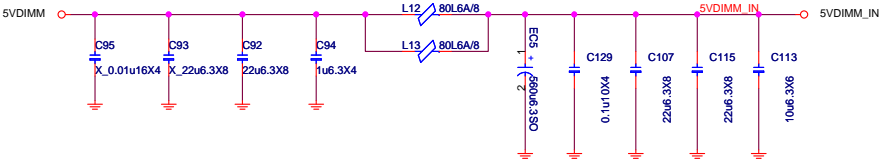
OCP = 7.925A*1.5=11.8875A
Current limit= 95.3K(R1054)*5uA/10/4mohm)=11.91A

2015.04.23 change to RT8231

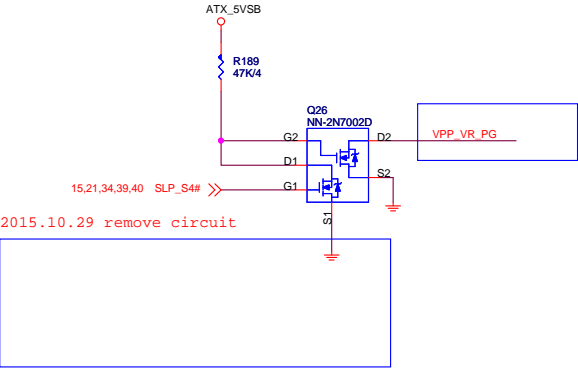
Vinafix.com

| VID | Reference Voltage (V) |
|-----|-----------------------|
| H | 0.675 |
| L | 0.75 |

$I_{rms} = I_{out} * \sqrt{((V_{out}/V_{in})) * (1 - (V_{out}/V_{in}))}$
 $= 7.925 * 0.42$
 $= 3.384A$

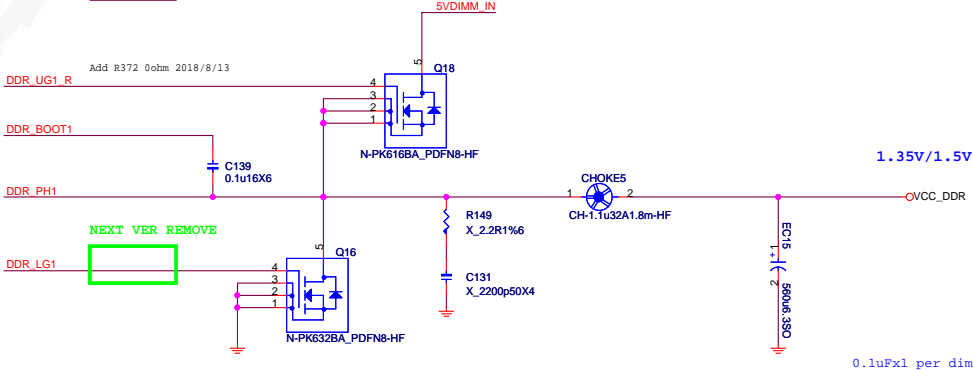
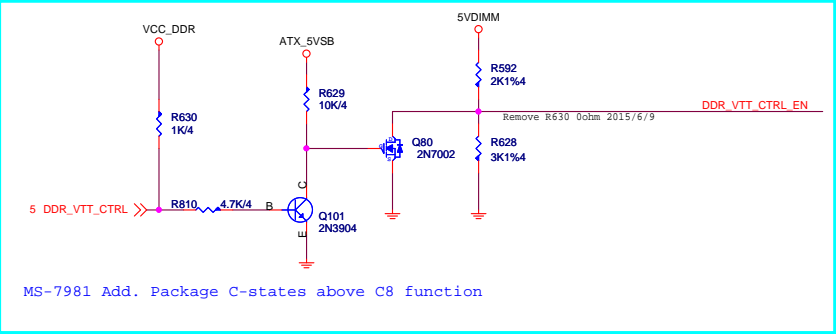


MAX: 7.925A
1.2V



2015.10.29 remove circuit

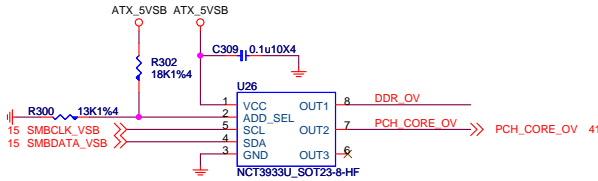
SLP_S4# de-assertion to VDDQ ramp down start
VPP ramp down after VDDQ ramp down




1.35V/1.5V

UPI VOLTAGE CONSOLE

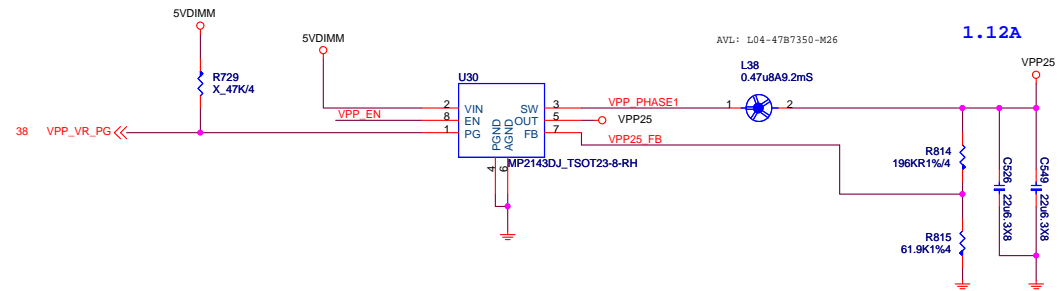
0x26 : RH=18K, RL=13K





| MICRO-STAR INT'L CO.,LTD | | |
|--------------------------|----------------------------|----------------|
| MS-7A15 | | |
| Size | Document Description | Rev |
| Custom | DDR-RT8231 | 10 |
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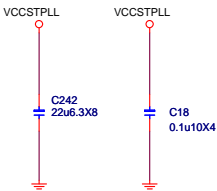
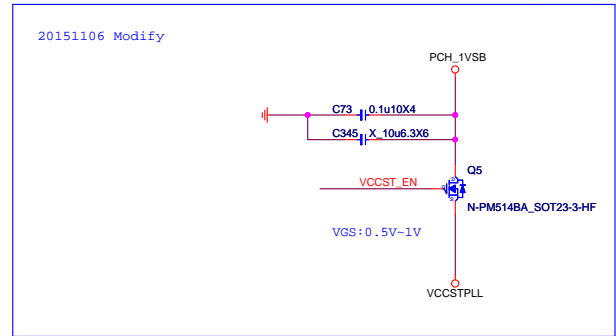
VPP25 Power
2.5V; 1.12A



VCCSTPLL

1.0V; VCCST:60mA,VCCPLL:150mA=60+150=210mA
For Cost down VCCST&VCCPLL merge

MAX: 210mA

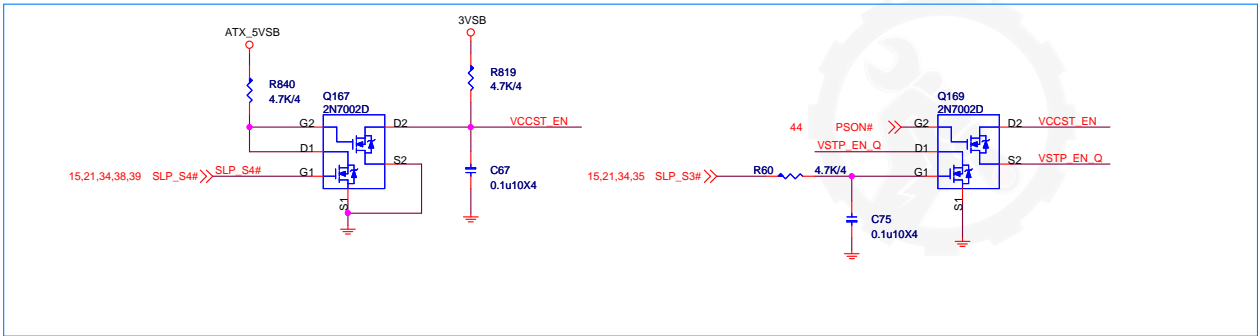


Main:D03-514BA09-N03
AVL:D03-0341409-A68,D03-P500209-N03 ?

VCCIO ramped and stable before
beginning of VCCOPC/VCCEPIO ramp

VCCST/PLL stable 1ms before PROCPWRGD

7981-2.2 modify 2015.05.28



MICRO-STAR INT'L CO.,LTD

MS-7A15

| | | |
|----------------------------------|---|-----------|
| Size Custom | Document Description CPU PWR_ST/PLL | Rev 10 |
| Date: Thursday, January 21, 2016 | Sheet 40 of 51 | |

PCH 1VSB

1.0V; 8.572A+5.5A+0.21A=14.282

OCp =21.423A

Rocset = 1.5 * I_{max} * R_{dson(LOW)} / I_{ocset}
 = 1.5 * 14.282 * 3.6mohm / 10uA
 =7.71K

Rocs:7.68K,OCp:

D03-4C05N03-005 : 15.36A

D03-632BA0C-N03 : 16.69A

when use UBIQ MOS Rocs:7.68K OCp:21.33A

R_{dson(LOW)} 4.5V

D03-4C05N03-005 : 5 mohm

D03-632BA0C-N03 : 4.6 mohm

D03-3116M00-U47 : 3.6mohm

2014.08.22 close to U34

2015.01.22
 for up1540:stuff R438->36K,
 C379->NC,C373->3.3nF
 for RT8125:R438.C379.C373->NC

2015.01.22
 for up1540:R403->2.2R,C362->1uF
 for RT8125:R403->10R,C362->1uF

20151103 Remove co-lay

close to PIN7

2014.12.25
 for up1540:C364&R407 ->NC

2014.12.25
 for up1540:C365 is OCP set min:5ohm
 stuff 7.87K OCP SET:15.74A
 RT8125C stuff C1000P C11-1022032-W08

2014.12.25
 for up1540:R623 ->NC

38 PCH_CORE_OV << PCH_CORE_OV

to sink/source over voltage IC.
 pin10 sink/source current capability can't over 1mA
 So max voltage can't over 1.8V.

from NCT3933

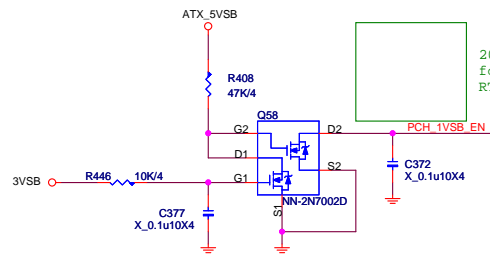
$$\begin{aligned} V_{out} &= V_{ref} * (1 + R_{821}/R_{822}) \\ &= 0.8 * (1 + 1K/3.24K) \\ &= 0.8 * 1.3086 \\ &= 1.047V \end{aligned}$$

$$\begin{aligned} I_{rms} &= I_{out} * \sqrt{(V_{out}/V_{in}) * (1 - (V_{out}/V_{in}))} \\ &= 10.664 * 0.4 \\ &= 4.2656A < 5000mA \end{aligned}$$

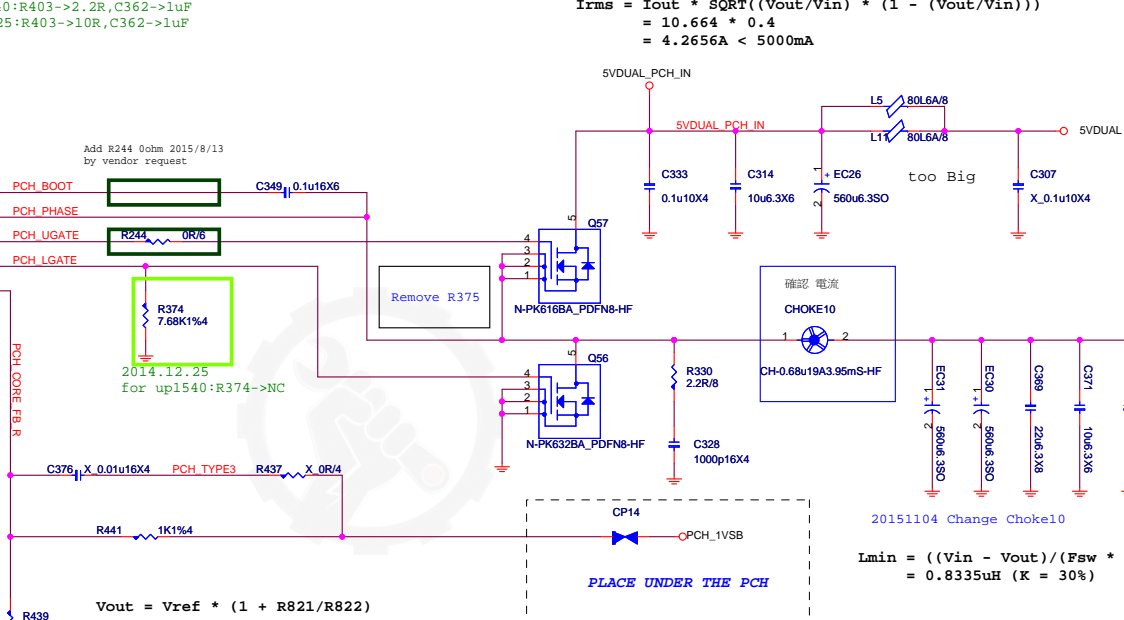
MAX:14.282A

20151104 Change Choke10

$$\begin{aligned} L_{min} &= ((V_{in} - V_{out}) / (F_{sw} * k * I_{out_max})) * (V_{out}/V_{in}) \\ &= 0.8335uH (K = 30\%) \end{aligned}$$



2014.12.25
 for up1540:R420 ->NC
 RT8125C:R420 ->NC



PLACE UNDER THE PCH



MICRO-STAR INT'L CO.,LTD

MS-7A15

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|----------------------------------|----------------------|-----|
| Custom | PCH Core power | 10 |
| Date: Thursday, January 21, 2016 | Sheet 41 of 51 | |

SA Power:1.05V,11.1A

$$OCP = 11.1A * 1.84 = 20.44A$$
$$\begin{aligned} R_{cs}(R15) &= OCP * R_{dson}(\text{Low side}) 2.5\text{mohm} / 10\text{uA} \\ &= 20.44 * (2.5)\text{mohm} / 10\text{uA} \\ &= 5.11\text{Kohm} \end{aligned}$$

Rocs:5.2836K,OCP:
D03-4C05N03-O05 : 15.76A
D03-632BA0C-N03 : 16.24A

Rocs:5.11K
when use UBIQ MOS :20.44A
Rdson(low)10V

| | |
|-----------------|-----------|
| D03-4C05N03-O05 | : 3.4mohm |
| D03-632BA0C-N03 | : 3.3mohm |
| D03-3056M00-U47 | : 4.2mohm |

2014.09.11 By layout

```
2014.12.25
for up1540:R214&R243 ->NC
```

```
SLP_S3# assertion to VR disabled
max:1us
```

EN:VIH2.4V
EN pin Maximum:6.5V

```
2015.01.22
for up1540:R96->2.2R,C84->1uF
for RT8125:R96->10R,C84->1uF
```

2014.10.16
up1540 no stuff

```
up1540 stuff R   
RT8125C stuff C1000P C11-1022032-W08
```

20151103 Remove co-lay

close to U35

```
2015.01.22
for up1540:stuff R223->36K,
C214->NC,C218->10nF
for RT8125:R223.C214.C218->NC
```

Add R232 0ohm 2015/8/13
by vendor request

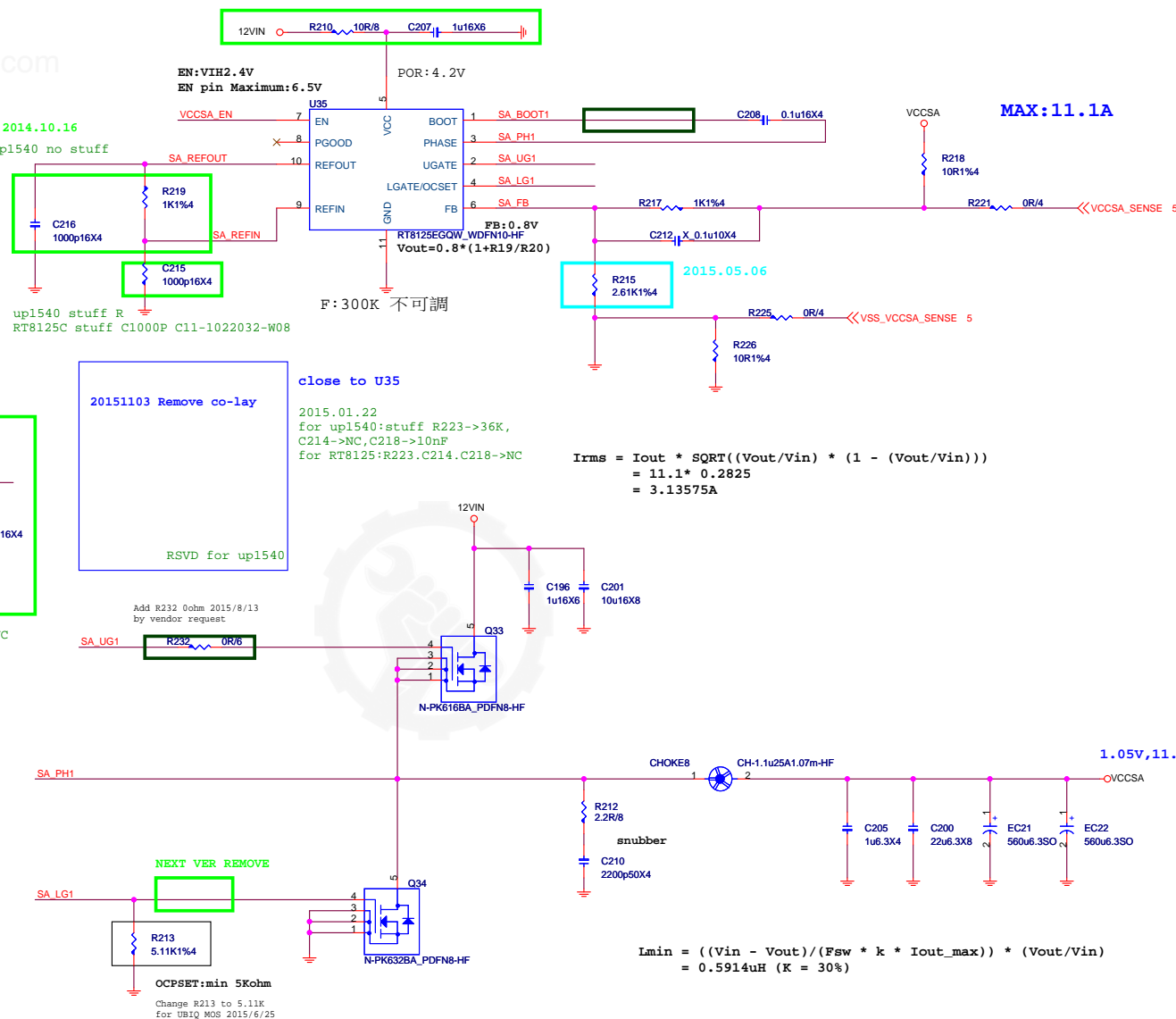
OCPSET:min 5Kohm
Change R213 to 5.11K
for UBIQ MOS 2015/6/25

```
Irms = Iout * SQRT((Vout/Vin) * (1 - (Vout/Vin)))
      = 11.1* 0.2825
      = 3.13575A
```

```
Lmin = ((Vin - Vout)/(Fsw * k * Iout_max)) * (Vout/Vin)
      = 0.5914uH (K = 30%)
```

MAX:11.1A

1.05V, 11.1A



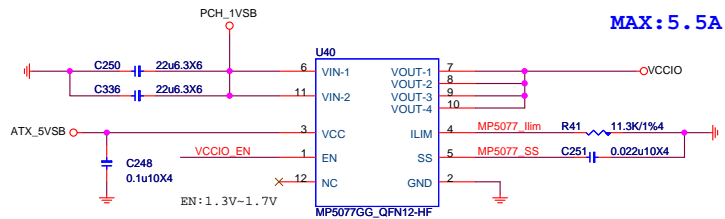
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| Size Custom | Document Description VCCSA - POWER RT8125E | Rev 10 |
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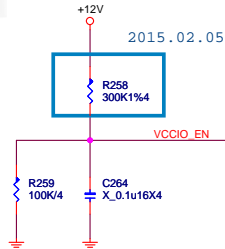
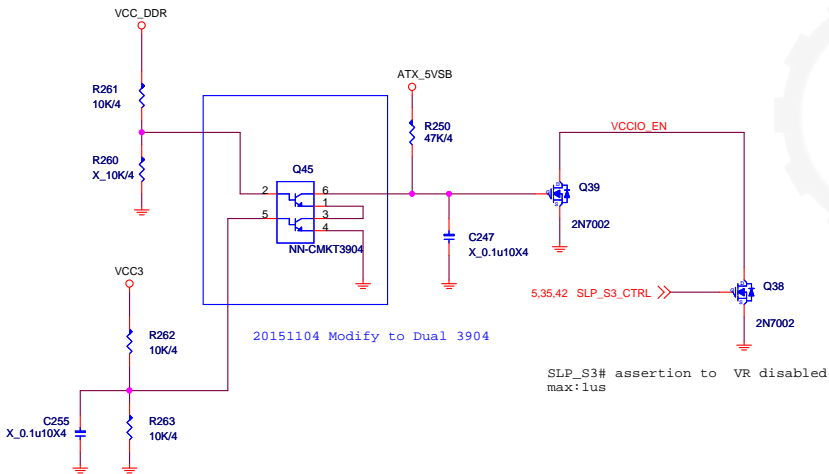
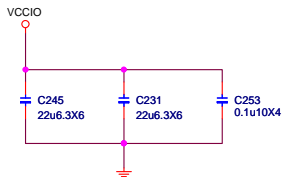
VCCIO

0.95V; 5.5A

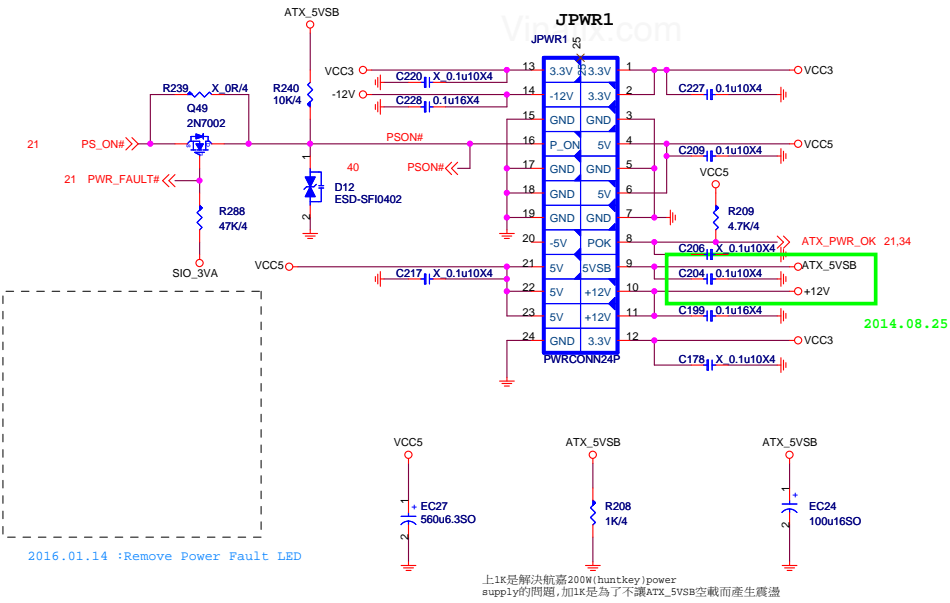


$$I_{limit} = (1/R_{limit}) * S, S = 80000, \text{ when } V_{IN} = 1V$$
$$= (1/11.3) * 80000 = 7.079A$$

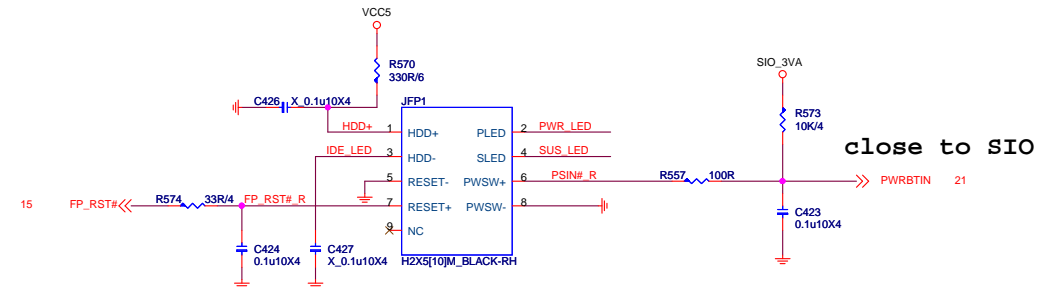
$$T_{ss} = (1/3) * ((V_{out} * C_{ss}) / I_{ss}), I_{ss} = 9uA$$
$$T_{ss} = (1/3) * ((1 * 22n) / 9uA) = 0.814ms$$



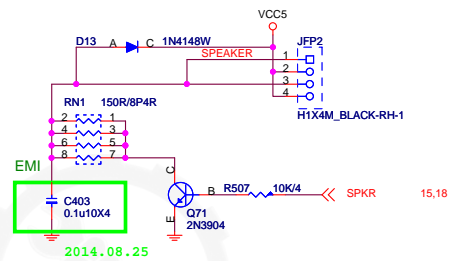
ATX POWER CONNECTOR



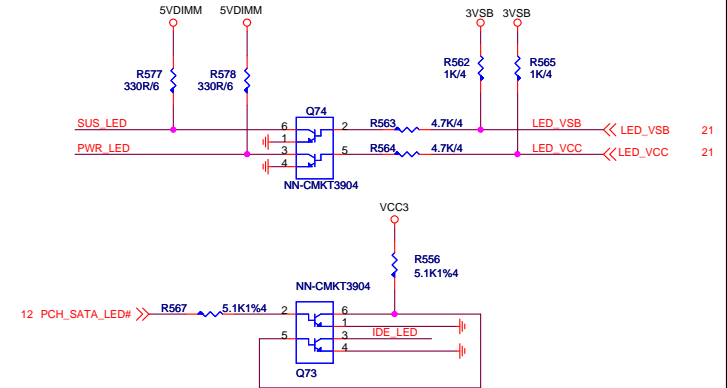
FRONT PANNEL



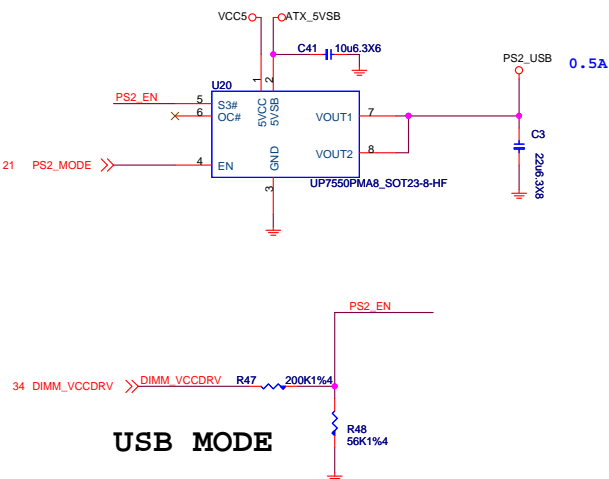
Speaker Pin Header



LED (for NV5533)



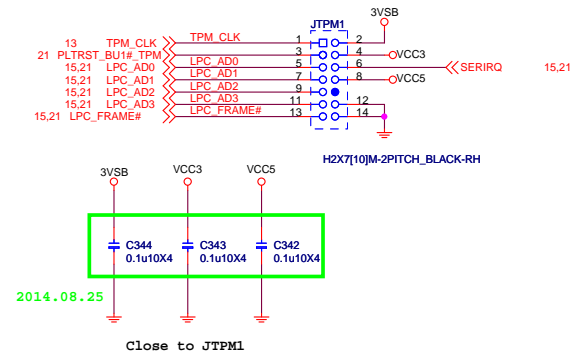
PS2 POWER



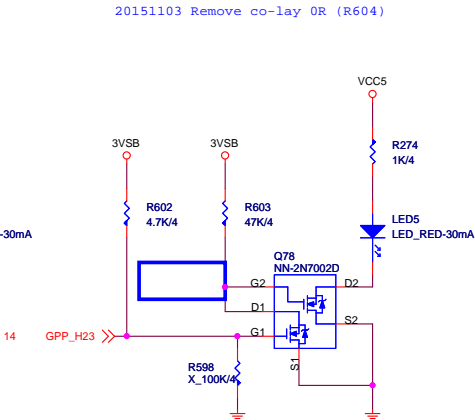
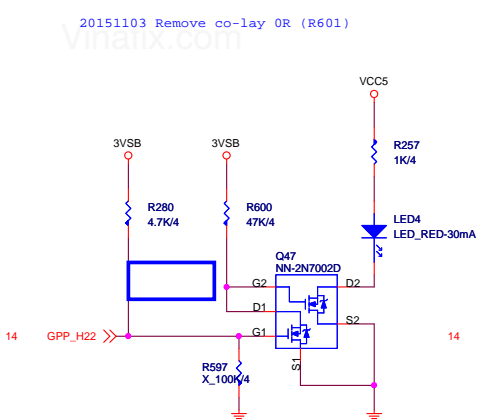
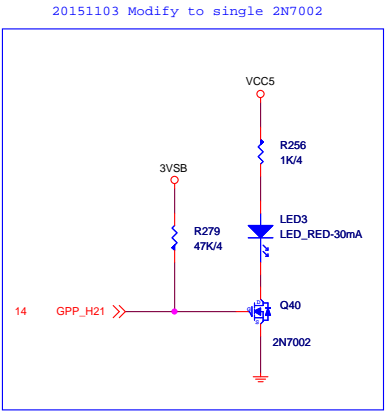
MSI LED

20151106 Remove MSI LED

TPM



DEBUG LED



| GPIO LED | GPP_H21 | GPP_H21 | GPP_H21 |
|-------------|------------------|----------------------------|----------------------------|
| 亮 | GPI PULL HIGH | GPO PO LOW | GPO PO LOW |
| 滅 | GPO LOW | GPO HIGH (default HIGH) | GPO HIGH (default HIGH) |

- 關機斷電狀態下，3個LED先維持default全暗，開機通電後：
1. 首先進行CPU checkCPU LED 亮，check PASS後則CPU LED滅掉。
 2. 接著依序進行Memory /memory LED亮check PASS後則memory LED滅掉。
 3. VGA的check/VGA LED亮，check PASS後則VGA LED滅掉。
 4. 因此最後正常順利開機後，三個LED燈都是滅掉的。（系統重啟或其他原因造成系統重開機，則LED仍按上述行為動作）

EMI CAP

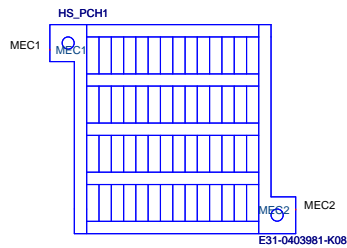
Vinafix.com



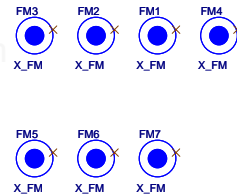
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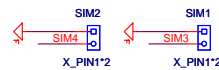
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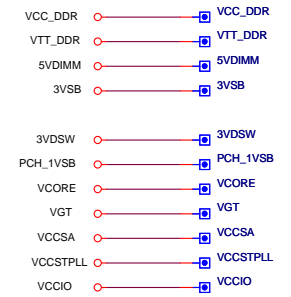
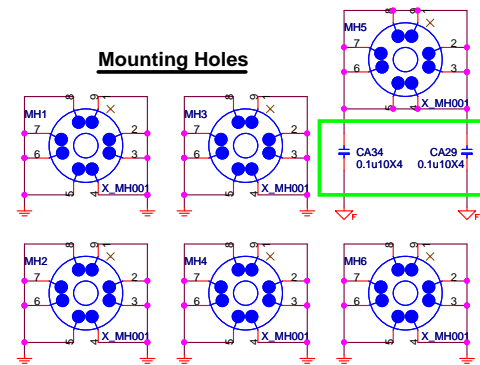
Optical Fiducial Marks-120



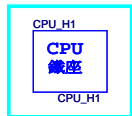
Simulation



Mounting Holes



20150423 PM Request cost down



PK0-07A1510-G37, 精成-深圳, 23, 寶安恩斯邁廠 (MSIS)
PK0-07A1510-E48, 競華, 23, 寶安恩斯邁廠 (MSIS)

| Model | Sample BOM | chipset | Market Name | BIOS Define |
|------------------|--------------|-----------------------|-------------|--------------|
| MS-7A15 | 601-7A15-01S | H110 chipset | DVI | E7A15ims.AXX |
| MS-7A15 OPT:A | 601-7A15-02S | H110 chipset OPT:A | HDMI | E7A15ims.AXX |

For BIOS BOM USE

| | GPP_G21 | GPP_G22 | GPP_G23 |
|------|---------|---------|---------|
| HDMI | 0 | 0 | 0 |
| DVI | 0 | 0 | 1 |

Reference